**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
ON APPEAL FROM THE EXAMINER TO THE BOARD
OF PATENT APPEALS AND INTERFERENCES**

In re Application of:	Robert A. Marshall et al.
Serial No.:	09/751,756
Filing Date:	December 29, 2000
Group Art Unit:	2614
Examiner:	Alexander Jamal
Confirmation No.:	5059
Title:	A METHOD AND SYSTEM FOR PROVIDING EXTENDED REACH OF A DIGITAL SUBSCRIBER LINE SIGNAL

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

APPEAL BRIEF

Appellants have appealed to this Board from the decision of the Examiner, contained in a Final Office Action mailed July 13, 2006 (the "*Final Office Action*"), finally rejecting Claims 1-3, 5-12, 14, and 16-26. Appellants mailed a Notice of Appeal on October 12, 2006. Appellants respectfully submit this Appeal Brief for consideration of the Board.

Real Party In Interest

This Application is currently owned by Cisco Technology, Inc. as indicated by:

an assignment recorded on 04/16/2001 from inventor Robert A. Marshall to Cisco Technology, Inc., in the Assignment Records of the PTO at Reel 011710, Frame 0008 (4 pages); and

an assignment recorded on 04/16/2001 from inventor Michael H. Capon to Cisco Technology, Inc., in the Assignment Records of the PTO at Reel 011710, Frame 0024 (7 pages).

Related Appeals And Interferences

The Appellants, the undersigned Attorney for Appellants, and the Assignee know of no applications on appeal that may directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

Status Of Claims

Claims 1-3, 5-12, 14, and 16-26 are pending; Claims 4, 13, and 15 are withdrawn; and Claims 1-3, 5-12, 14, and 16-26 are rejected by the *Final Office Action*. Appellants present all pending claims, Claims 1-3, 5-12, 14, and 16-26, for consideration by the Board on appeal.

Status of Amendments

In Appellants' September 13, 2006 Response to the *Final Office Action*, Appellants amended Claims 1, 11, 16, 18, and 19 to remove unnecessary limitations added by a previous response. In an Advisory Action dated September 28, 2006 ("*Advisory Action*"), the Examiner entered these amendments.

Accordingly, all amendments submitted by Appellants have been entered by the Examiner.

Summary of Claimed Subject Matter

Embodiments of the present invention and its advantages are best understood by referring to FIGURES 1 through 5 of the drawings, like numerals being used for like and corresponding parts of the various drawings. (Page 7, lines 2-5).

FIGURE 1 is a block diagram of a system 10 for providing a DSL signal from a central office 18 to a customer's premises 20. A DSL signal travels over telephone lines 16, utilizing higher frequencies for data signals than those used for voice signals. As described above, one problem associated with digital subscriber line technology is that the data signal degrades over the telephone line 16. This occurs both because of attenuation on telephone line 16 especially at higher frequencies and due to crosstalk between adjacent telephone wires 16. Due to this degradation the maximum distance between the customer's premises 20 and a central office for customary implementations of digital subscriber line technology is approximately three miles. (Page 7, lines 6-19).

According to the teachings of the invention, this distance is increased by providing a repeater and amplifier that collects and retransmits a digital subscriber line signal at various points between central office 18 and the customer premises 20. Details of example embodiments of a method and system for extending the reach of such a DSL signal are described in conjunction with FIGURES 2A through 6. (Page 7, lines 20-27).

FIGURE 2A is a block diagram of a system 100 for extending the reach of a DSL signal according to the teachings of the invention, and FIGURE 2B is a block diagram of a system 200 for extending the reach of a DSL signal according to another embodiment of the invention. As shown, bi-directional repeater amplifier 22 is placed between customer premises 20 and the central office 18. This allows extension of the reach of the DSL signal by approximately another three miles. (Page 7, line 28 - Page 8, line 4).

FIGURE 2B shows a plurality of bi-directional repeater amplifiers 22 used to extend the reach of a DSL signal. In this example, customer premises 20 may be located approximately 6 miles from central office 18, but decreased spacing is utilized between the bi-directional repeater amplifiers to provide a higher data transmission rate. (Page 8, lines 5-11).

FIGURE 3 is a flowchart illustrating an example method for extending the reach of a DSL signal. The method begins at step 302. At step 304 an incoming signal is received over

telephone lines 16. According to one embodiment of the invention, suitable circuitry is utilized such that the reach of both upstream and downstream signals are extended. In such an embodiment, step 304 of receiving the signal may include an additional step of determining whether the signal is upstream or downstream and transmitting it in an appropriate direction to suitable circuitry for processing. (Page 8, lines 12-23).

At a step 306, a received signal that requires amplification is split into voice and data bands. As described above, a DSL signal may comprise a voice band of zero to approximately 4 kilohertz and a data band of approximately 25 kilohertz to 1.1 megahertz for transmission of data signals. Alternatively, a DSL signal may include only data with no voice signal. In such a case, step 306 is not utilized. (Page 8, lines 24-31).

Certain forms of DSL discriminate between upstream and downstream transmissions. For example, according to ADSL, the frequency range of approximately 25 kilohertz to 271 kilohertz is utilized for upstream transmissions and the frequency range of approximately 271 kilohertz to 1.1 megahertz is utilized for downstream transmissions. (Page 9, lines 1-6).

Once the DSL signal is split into voice and data bands, the data signal is conditioned to acquire underlying data and to transmit it in a regenerated form. Such a procedure contrasts with simply amplifying the DSL signal at this point in that such amplification will also amplify any associated noise, resulting in poor signal quality. Such signal conditioning is performed by steps 308, 310, and 312. (Page 9, lines 7-14).

At step 308, the data signal is demodulated. According to one embodiment, such demodulation may include converting the data signal from analog format to digital format and performing a Fast Fourier Transform on the digital signal to form a plurality of frequency bands of data. (Page 9, lines 15-20).

At a step 310, the demodulated data signal is recovered. Recovery of the demodulated data signal refers to determining true values for each of the data bits stored in the plurality of data bins. According to one embodiment, this step involves determining a constellation that is associated with each bit and setting the value of the bit to the ideal value of the constellation. This step may also be referred to as requantization. (Page 9, lines 21-29).

At a step 312, requantized data is remodulated. Such remodulation may include an Inverse Fast Fourier Transform to produce a digital signal in the time domain rather than the requantized data generated at step 310, which is in the frequency domain. In addition, the

resulting digital signal in the time domain may be converted to analog form for subsequent amplification. (Page 9, line 30 - Page 10, line 4).

At step 314, the remodulated analog signal representing the data of the DSL signal is amplified. In addition, the voice signal split out at step 306 is also amplified. The amount of amplification is a function of the amount of loss that occurs over telephone lines 16 and the associated circuitry, such as the signal director described below. (Page 10, lines 5-11).

At step 316, the amplified voice and data signals are recombined into a single data signal. This combination step may also include amplifying the combined signal. (Page 10, lines 12-15).

At step 318, the recombined and amplified voice and data signals are retransmitted along telephone lines 16 to customer premises 20, central office 18, or another bi-directional repeater amplifier 22. (Page 10, lines 16-19).

The method concludes at step 320. (Page 10, line 20).

Thus, according to the teachings of the invention, the reach of a DSL signal may be extended by acquiring the underlying data signal by determining the true values associated with that data signal and then requantizing that data for subsequent amplification and re-transmittal. By extending the reach of the DSL signal, widespread use of DSL technology may be deployed, allowing remote areas that heretofore have not had access to such technology to benefit from it. The method of FIGURE 3 may be implemented in many forms. Examples of such implementation are described in FIGURES 4 through 5. (Page 10, lines 21-31).

FIGURE 4 is a circuit diagram of one implementation of bi-directional repeater amplifier 22. In this example, either an upstream or a downstream DSL signal may be received by bi-directional repeater amplifier 122 and that signal is transmitted according to the teachings of the invention in the appropriate direction. (Page 11, lines 1-6).

Bi-directional repeater amplifier 122 comprises a pair of signal directors 128, 130. Signal director 128 receives an upstream signal 127 sent from customer premises 20 along lines 16 and directs signal 127 to a conditioning circuit 202 as signal 139. Signal director 128 also receives a downstream signal 131, which has been amplified according to the teachings of the invention, and directs signal 131 toward customer premises 20 along line 16. Thus, signal director 128 directs incoming and outgoing signals appropriately along telephone lines 16. Signal director 130 operates similarly, receiving a downstream signal

133 and also receiving an amplified signal 135 and directs these signals appropriately. (Page 11, lines 7-19).

In this example, signal directors 128, 130 are balanced bridges. However, signal directors 128, 130 may be formed by a variety of circuits operable to receive signals in two directions and to direct them along the appropriate path, including a resistance bridge, transformer or other hybrid circuit. (Page 11, lines 20-25).

Bi-directional repeater amplifier 122 may also include a pair of switches 125 and 165 to disable operation of the bi-directional receiver amplifier 122. Use of a fail-safe mode associated with repeater 122 allowing voice transmissions or reduced data rate transmissions may be incorporated. Such a fail-safe mode would deactivate the repeater 122 and switch it out of line using switches 125 and 165. (Page 11, line 26 - Page 12, line 2).

Also associated with bi-directional receiver amplifier 122 is a controller 124. Controller 124 controls settings associated with functions performed by data acquirer and retransmitter 140 and 154, as described below. Controller 124 may also be used for diagnostic purposes. Bi-directional receiver amplifier 122 also includes a power supply 126 that provides suitable power levels to bi-directional receiver amplifier 122. These power levels may include, in one example, a 5 volt voltage level produced from a 130 volt level at central office 18. In such embodiments, communication of power from central office 18 to power supply 126 may occur over lines separate from telephone lines 16 (not explicitly shown), or in some embodiments, over lines 16, which may result in loss of voice signals over these telephone lines 16. (Page 12, lines 3-18).

Once a signal is received at one of the signal directors 128, 130, the signal is directed to one of two conditioning circuits 202, 204. The operation of each of the conditioning circuits 202, 204 is substantially the same. Conditioning circuit 202 is described as an example. (Page 12, lines 19-24).

Conditioning circuit 202 receives a DSL signal 139, which is substantially similar to signal 127. DSL signal 139 is received by conditioning circuit 202 and a regenerated version of that signal is produced as signal 135 by conditioning circuit 202. According to the teachings of the invention, signal 135 is an amplified version of the DSL signal 139, but it more accurately reflects the original underlining data. According to this embodiment, conditioning circuit 202, generally, filters DSL signal 139, demodulates, requantizes, remodulates the data signal, and amplifies both the voice and data signals before combining

the audio and data signals for retransmission at signal 135. In other embodiments, only data is transmitted and amplified, with no associated voice signal. Example circuitry associated with conditioning circuit 202 is described below. (Page 12, line 25 - Page 13, line 8).

Conditioning circuit 202 includes a switch 145, a low band filter 146, an audio amplifier 148, a band pass filter 138, a data acquirer and re-transmitter 140, a data amplifier 142, and a summer/amplifier 144. Low pass filter 146 and audio amplifier 148 are associated with any voice signal contained in DSL signal 139. High band filter 138, data acquirer and transmitter 140, and data amplifier 142 are associated with the data signal contained within DSL signal 131. (Page 13, lines 9-17).

Switch 145 may be open for SDSL operations. With SDSL, only data is transmitted, with no associated voice signal. Therefore, there is no need for amplification of the voice signal. When switch 145 is closed, low pass filter 146 allows passage of the low frequency signals, corresponding to voice signals, of DSL signal 139. According to one embodiment of the invention, the corner frequency for low band filter 146 is four kilohertz. (Page 13, lines 18-25).

In this embodiment, band pass filter 138, corresponding to upstream transmissions, allows passage of frequencies between approximately 25 to approximately 272 kilohertz and band pass filter 152, corresponding to downstream transmissions, allows passage of frequencies between approximately 272 kilohertz and 1.1 megahertz; however, other suitable frequency ranges may be used to divide portions of DSL signal 139 as desired. Band pass filter 138 produces a filtered signal 149. Filtered signal 149 is received by data acquirer and re-transmitter 140. Data acquirer and re-transmitter 140 perform a number of functions to produce a requantized signal 141 that is representative of the original data associated with DSL signal 127. Circuitry associated with data acquirer and re-transmitter 140 for performing these functions are described in greater detail in FIGURE 5. (Page 13, line 26 - Page 14, line 10).

Audio amplifier 148 amplifies the low band signal 151 received from low band filter 146 and data amplifier 142 amplifies the requantized high band signal 141. The amount of amplification for both data amplifier 142 and audio amplifier 148 may be determined based upon the amount of loss associated with transmission of the DSL signal over telephone lines 16 and the distance between bi-directional repeater amplifier 122 and the associated central office or customer premises. (Page 14, lines 11-19).

The outputs of both data amplifier 142 and audio amplifier 148 are received by summer/amplifier 144. Summer/amplifier 144 combines the amplified audio signal received from audio amplifier 148 and the requantized and amplified data signal received from data amplifier 142 into a single amplified DSL signal 135. Amplified DSL signal 135 is received by signal director 130 and transmitted to central office 18 by signal director 130 as described above. (Page 14, lines 20-28).

Thus, according to the teachings of the invention, a DSL signal may be amplified to allow greater reach of the DSL signal. (Page 14, lines 29-31).

Conditioning circuit 204 is substantially similar to conditioning circuit 202 and includes a band pass filter 152, a data acquirer and re-transmitter 154, a data amplifier 156, a switch 163, a low band filter 160, an audio amplifier 162, and a summer/amplifier 158. Conditioning circuit 204 operates in substantially the same manner as conditioning circuit 202. As described above, band pass filter 152 may differ somewhat from band pass filter 138 for implementations where DSL data are transferred in different frequency bands depending on whether the transmission is upstream or downstream; however, the principles of splitting the voice and data signals into separate bands are the same. (Page 15, lines 1-13).

Additional details of one embodiment data acquirer and re-transmitter 140 and data acquirer and re-transmitter 154 are described below in conjunction with FIGURE 5. (Page 15, lines 14-17).

FIGURE 5 is a block diagram of one example of data acquirer and re-transmitter 140. Data acquirer and re-transmitter 140 includes analog-to-digital converter 262, a Fast Fourier Transformer 264, a requantizer 266, an Inverse Fast Fourier Transformer 268, and a digital-to-analog converter 270. Analog-to-digital converter 262 receives analog data signal 149. Once the signal is converted to digital form, it is provided to Fast Fourier Transformer 264. Fast Fourier Transformer 264 divides the received digital signal into a plurality of frequency ranges and also discards data in undesired frequency ranges. Fast Fourier Transformer 264 may be implemented in software or by suitable circuitry. In one example, a digital signal processor (DSP) is utilized. In this embodiment, for upstream data transmissions, frequency ranges that exceed approximately 272 kilohertz and fall below 25 kilohertz are discarded because these ranges are outside the ranges in which data are transferred according to DSL technology. For downstream transmissions, frequencies outside the range of 272 kilohertz to 1.1 megahertz are discarded. (Page 15, line 18 - Page 16, line 6).

Fast Fourier Transformer 264 generates appropriate bins of data on line 265 for receipt by requantizer 266. In this embodiment, for upstream transmissions, frequency bins corresponding to bins 5 through 63 commonly used in DMT ADSL technology are generated; for downstream transmissions, frequency bins corresponding to bins 64 through 255 are generated. (Page 16, lines 7-13).

Requantizer 266 receives the frequency domain data on line 265 from Fast Fourier Transformer 264. Requantizer 266 determines for each bin received, a symbol associated with the data bit. The symbol refers to one of a discrete number of possible data sequences that the received data could be intended to represent. The active constellations are determined and specified by controller 124. For each bin, requantizer 266 assigns the value of the closest symbol to that bin. Requanitization is performed in the frequency domain. Requantizer 266 generates a frequency domain signal and provides that signal over line 267 to inverse Fast Fourier Transformer 268. This signal on line 267 includes requantized data in bins associated with bins received along line 265. For bins not received along line 265, the associated values are set to zero. (Page 16, lines 14-29).

Inverse Fast Fourier Transformer 268 converts the requanitized frequency domain signal to a time domain signal digital signal and provides the time domain digital signal to digital-to-analog converter 270. Inverse Fast Fourier Transformer 268 may be implemented by software or suitable circuitry. In one example, a digital signal processor (DSP) is utilized. Digital-to-analog converter 270 generates analog signal 141 for providing to data amplifier 142, as described above in FIGURE 4. (Page 16, line 30 - Page 17, line 8).

Thus, by requantizing the data associated with DSL signal 129, errors resulting from transmission over long lines are reduced, allowing subsequent amplification of data more representative of the true data values, rather than amplification of associated noise. This allows DSL signals to be retransmitted, resulting in increased reach of DSL signals and more widespread deployment of DSL technology. (Page 17, lines 8-15).

Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions, and alterations can be made therein without departing from the spirit and scope of the present invention as defined by the appended claims. (Page 17, lines 16-21).

With regard to the independent claims currently under Appeal, Appellants provide the following concise explanation of the subject matter recited in the claim elements. For brevity, **Appellants do not necessarily identify every portion of the Specification and drawings relevant to the recited claim elements**. Additionally, this explanation should not be used to limit Appellants' claims but is intended to assist the Board in considering the Appeal of this Application.

For example, independent Claim 1 recites the following:

A method for providing greater reach of a DSL signal comprising: (*see, e.g.*, Fig. 3; page 8, lines 12-13; page 9, lines 7-14)

receiving an incoming DSL signal including a data signal; (*see, e.g.*, page 8, lines 14-23; page 12, lines 25-32)

demodulating the data signal; (*see, e.g.*, page 9, lines 15-20; page 15, line 23 - page 16, line 13)

requantizing the demodulated data signal by determining a constellation associated with each bit of data in the modulated data signal and resetting the value of that bit to the value of the constellation to acquire underlying data in the data signal and transform the data signal into a regenerated form; (*see, e.g.*, page 9, lines 21-29; page 16, line 14 - page 17, line 7)

modulating the requantized data signal; (*see, e.g.*, page 9, line 30 - page 10, line 4; page 16, line 30 - page 17, line 7)

amplifying the modulated requantized data signal; and (*see, e.g.*, page 10, line 5-11; page 14, lines 11-28)

transmitting the amplified signal. (*see, e.g.*, page 10, lines 16-19; page 14, lines 25-28)

As another example, independent Claim 11 recites the following:

A method for providing greater reach of a DSL signal having a data portion, comprising: (*see, e.g.*, Fig. 3; page 8, lines 12-31; page 9, lines 7-14)

demodulating the data portion; (*see, e.g.*, page 9, lines 15-20; page 15, line 23 - page 16, line 13)

requantizing the demodulated data portion by determining a constellation associated with each bit of data in the modulated data portion and resetting the value of that bit to the value of the constellation to acquire underlying data in the data portion and transform the data portion into a regenerated form; (*see, e.g.*, page 9, lines 21-29; page 16, line 14 - page 17, line 7)

modulating the requantized data portion; (*see, e.g.*, page 9, line 30 - page 10, line 4; page 16, line 30 - page 17, line 7)

amplifying the modulated requantized data portion; and (*see, e.g.*, page 10, lines 5-11; page 14, lines 11-28)

transmitting the amplified modulated requantized data portion. (*see, e.g.*, page 10, lines 16-19; page 14, lines 25-28)

As another example, independent Claim 16 recites the following:

A system for facilitating greater reach of a DSL signal having a data portion, comprising: (*see, e.g.*, Fig. 1; Fig. 4; Fig. 5; page 7, lines 20-27; page 8, lines 12-31; page 9, lines 7-14)

a means for demodulating the data portion; (*see, e.g.*, page 9, lines 15-20; page 15, line 23 - page 16, line 13)

a means for requantizing the demodulated data portion by determining a constellation associated with each bit of data in the modulated data portion and resetting the value of that bit to the value of the constellation and transform the data portion into a regenerated form; (*see, e.g.*, page 9, lines 21-29; page 16, line 14 - page 17, line 7)

a means for modulating the requantized data portion; and (*see, e.g.*, page 9, line 30 - page 10, line 4; page 16, line 30 - page 17, line 7)

a means for amplifying the modulated requantized data portion. (*see, e.g.*, page 10, lines 5-11; page 14, lines 11-19)

As another example, independent Claim 18 recites the following:

A system for facilitating providing greater reach of a DSL signal comprising: (*see, e.g.*, Fig. 1; Fig. 4; Fig. 5; page 7, lines 20-27; page 11, lines 1-6)

a means for splitting the DSL signal into separate voice and data signals; (*see, e.g.*, page 8, lines 24-31; page 12, lines 19-24; page 13, line 9 - page 14, line 7)

a means for demodulating the data signal; (*see, e.g.*, page 9, lines 15-20; page 15, line 23 - page 16, line 13)

a means for requantizing the demodulated data signal by determining a constellation associated with each bit of data in the modulated data signal and resetting the value of that bit to the value of the constellation and transform the data signal into a regenerated form; (*see, e.g.*, page 9, lines 21-29; page 16, line 14 - page 17, line 7)

a means for modulating the requantized data signal; and (*see, e.g.*, page 9, line 30 - page 10, line 4; page 16, line 30 - page 17, line 7)

a means for combining and amplifying the voice and data signals into a combined signal. (*see, e.g.*, page 10, lines 5-15; page 14, lines 11-28)

As another example, independent Claim 19 recites the following:

A bi-directional DSL repeater and amplifier comprising: (*see, e.g.*, Fig. 4, item 122; page 11, lines 1-6)

a first signal detector operable to receive a first incoming DSL signal including a first data signal and direct the first incoming DSL signal to a first conditioning circuit and also operable to receive a first outgoing data signal from a second conditioning circuit and direct the first outgoing data signal over a first telephone line; (*see, e.g.*, Fig. 4, items 128 and 130; page 8, lines 14-23; page 11, lines 7-25; page 12, lines 25-32)

the first conditioning circuit being operable to: (*see, e.g.*, Fig. 4, items 202 and 204; page 12, lines 19-24)

receive a signal indicative of the first incoming DSL signal; (*see, e.g.*, page 8, lines 14-23; page 12, lines 25-32)

demodulate, requantize, and remodulate the first data signal to produce a first remodulated data signal, the first data signal requantized by determining a constellation associated with each bit of data in the modulated first data signal and resetting the value of that bit to the value of the constellation to acquire underlying data in the first data signal and transform the first data signal into a regenerated form; and (*see, e.g.*, page 9, line 15 - page 10, line 4; page 12, line 32 - page 13, line 8; page 15, line 23 - page 17, line 7)

amplify the first remodulated data signal to produce a second outgoing data signal; (*see, e.g.*, page 10, lines 5-11; page 14, lines 11-28)

the second conditioning circuit being operable to: (*see, e.g.*, Fig. 4, items 202 and 204; page 12, lines 19-24)

receive a signal indicative of a second incoming DSL signal including a second data signal; (*see, e.g.*, page 8, lines 14-23; page 12, lines 25-32)

demodulate, requantize, and remodulate the second data signal to produce a second remodulated data signal, the second data signal requantized by determining a constellation associated with each bit of data in the modulated data signal and resetting the value of that bit to the value of the constellation to acquire underlying data in the second data signal and transform the second data signal into a regenerated form; and (*see, e.g.*, page 9, line 15 - page 10, line 4; page 12, line 32 - page 13, line 8; page 15, line 23 - page 17, line 7)

amplify the second remodulated data signal to produce the first outgoing data signal; and (*see, e.g.*, page 10, lines 5-11; page 14, lines 11-28)

a second signal detector operable to receive the second incoming DSL signal and direct the second incoming DSL signal to the second conditioning circuit and also operable to receive the second outgoing data signal from the first conditioning circuit and direct the second outgoing data signal over a second telephone line. (*see, e.g.*, Fig. 4, items 128 and 130; page 8, lines 14-23; page 11, lines 7-25; page 12, lines 25-32)

As another example, dependent Claim 3 recites the following:

The method of Claim 1, wherein demodulating the data signal comprises:

converting the data signal from analog to digital form;

dividing, by a Fast Fourier Transformer, the data signal in digital form into a plurality of desired data bins specified by frequency; and

discarding data outside the plurality of desired data bins. (*see, e.g.*, Figure 3, step 308; page 9, lines 15-20; page 15, line 23 - page 16, line 13)

As another example, dependent Claim 5 recites the following:

The method of Claim 1, wherein modulating the requantized data signal comprises combining, by an inverse Fast Fourier Transformer, a plurality of requantized data in a plurality of data bins specified by frequency into a digital signal in the time domain and converting the digital signal in the time domain to an analog signal. (*see, e.g.*, Figure 3, step 312; page 9, line 30 - page 10, line 4; page 16, line 30 - page 17, line 7)

As another example, dependent Claim 17 recites the following:

The system of Claim 16, and further comprising a means for transmitting the amplified modulated requantized data portion. (*see, e.g.*, Figure 4, items 16, 18, 20, 22, 128, 130; page 10, lines 16-19; page 14, lines 25-28)

As another example, dependent Claim 22 recites the following:

The bi-directional DSL repeater and amplifier of Claim 19, wherein the first conditioning circuit comprises on analog-to-digital converter and a Fast Fourier Transformer for demodulating the first data signal. (*see, e.g.*, Figure 5, items 262 and 264; page 9, lines 15-20; page 15, line 23 - page 16, line 13)

As another example, dependent Claim 23 recites the following:

The bi-directional DSL repeater and amplifier of Claim 19, wherein the first conditioning circuit comprises a digital-to-analog converter and an Inverse Fast Fourier Transformer for converting the first data signal into digital format. (*see, e.g.*, Figure 5, items 270 and 268; page 9, line 30 - page 10, line 4; page 16, line 30 - page 17, line 7)

Grounds Of Rejection To Be Reviewed On Appeal

Are Claims 1, 3, 5-6, and 11-12, 14, 16-17 unpatentable over U.S. Patent No. 6,236,664 issued to Erreygers ("*Erreygers*") in view of U.S. Patent No. 6,088,385 issued to Liu ("*Liu*")?

Are Claims 18-25 unpatentable over *Erreygers* in view of *Liu* in further view of U.S. Patent No. 6,658,049 issued to McGhee et al. ("*McGhee*")?

Are Claims 2, 7, and 8 unpatentable over *Erreygers* in view of *Liu* in further view of *McGhee*?

Are Claims 9 and 10 unpatentable over *Erreygers* in view of *Liu* in further view of U.S. Patent No. 4,878,232 issued to Fisher ("*Fisher*")?

Is Claim 26 unpatentable over *Erreygers* in view of *Liu* in further view of *McGhee* in further view of *Fisher*?

Argument

I. 35 U.S.C. § 103(a) Rejections: All claims are patentable over the various proposed combinations of *Erreygers*, *Liu*, *McGhee*, and *Fisher*.

The Examiner rejects Claims 1-3, 5-12, 14, and 16-26 under 35 U.S.C. § 103(a) as being unpatentable over various combinations of U.S. Patent No. 6,236,664 issued to Erreygers ("*Erreygers*"), U.S. Patent No. 6,088,385 issued to Liu ("*Liu*"), U.S. Patent No. 6,658,049 issued to McGhee et al. ("*McGhee*"), and U.S. Patent No. 4,878,232 issued to Fisher ("*Fisher*").[1] Copies of *Erreygers*, *Liu*, *McGhee*, and *Fisher* are attached in the Evidence Appendix. For the reasons discussed below, Appellants respectfully submit that these rejections are improper and should be reversed by the Board.

A. Standard

The question raised under 35 U.S.C. § 103 is whether the prior art taken as a whole would suggest the claimed invention taken as a whole to one of ordinary skill in the art at the time of the invention. *See* 35 U.S.C. § 103(a). Accordingly, even if all elements of a claim are disclosed in various prior art references, which is certainly not the case here as discussed below, the claimed invention taken as a whole cannot be said to be obvious without some reason given in the prior art why one of ordinary skill in the art at the time of the invention would have been prompted to modify the teachings of a reference or combine the teachings of multiple references to arrive at the claimed invention.

The M.P.E.P. sets forth the strict legal standard for establishing a *prima facie* case of obviousness based on modification or combination of prior art references. "To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally

[1] Specifically, the Examiner rejects: (1) Claims 1, 3, 5-6, and 11-12, 14, 16-17 as unpatentable over *Erreygers* in view of *Liu*, (2) Claims 18-25 as unpatentable over *Erreygers* in view of *Liu* in further view of *McGhee*, (3) Claims 2, 7, and 8 as unpatentable over *Erreygers* in view of *Liu* in further view of *McGhee*, (4) Claims 9 and 10 as unpatentable over *Erreygers* in view of *Liu* in further view of *Fisher*, and (5) Claim 26 as unpatentable over *Erreygers* in view of *Liu* in further view of *McGhee* in further view of *Fisher*. (*Final Office Action*, pages 2, 5, 7, and 8).

available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references where combined) must teach or suggest all the claim limitations." M.P.E.P. § 2142, 2143. The teaching, suggestion or motivation for the modification or combination and the reasonable expectation of success must both be found in the prior art and cannot be based on an Appellant's disclosure. *See Id.* (citations omitted). "Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art" at the time of the invention. M.P.E.P. § 2143.01. Even the fact that references *can* be modified or combined does not render the resultant modification or combination obvious unless the prior art teaches or suggests the desirability of the modification or combination. *See Id.* (citations omitted). Moreover, "To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. All words in a claim must be considered in judging the patentability of that claim against the prior art." M.P.E.P. § 2143.03 (citations omitted).

The governing Federal Circuit case law makes this strict legal standard even more clear.[2] According to the Federal Circuit, "a showing of a suggestion, teaching, or motivation to combine or modify prior art references is an essential component of an obviousness holding." *In re Sang-Su Lee*, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433 (Fed. Cir. 2002) (quoting *Brown & Williamson Tobacco Corp. v. Philip Morris Inc.*, 229 F.3d 1120, 1124-25, 56 U.S.P.Q.2d 1456, 1459 (Fed. Cir. 2000)). "Evidence of a suggestion, teaching, or motivation . . . may flow from the prior art references themselves, the knowledge of one of ordinary skill in the art, or, in some cases, the nature of the problem to be solved." *In re Dembiczak*, 175 F.3d 994, 999, 50 U.S.P.Q.2d 1614, 1617 (Fed. Cir. 1999). However, the "range of sources available . . . does not diminish the requirement for actual evidence." *Id.* Although a prior art device "may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in the reference to do so." *In re Mills*, 916 F.2d at 682, 16 U.S.P.Q.2d at 1432. *See also In re Rouffet,* 149 F.3d 1350, 1357, 47

[2] Note M.P.E.P. 2145 X.C. ("The Federal Circuit has produced a number of decisions overturning obviousness rejections due to a lack of suggestion in the prior art of the desirability of combining references.").

U.S.P.Q.2d 1453, 1457-58 (Fed. Cir. 1998) (holding a *prima facie* case of obviousness not made where the combination of the references taught every element of the claimed invention but did not provide a motivation to combine); *In Re Jones*, 958 F.2d 347, 351, 21 U.S.P.Q.2d 1941, 1944 (Fed. Cir. 1992) ("Conspicuously missing from this record is any evidence, other than the PTO's speculation (if that can be called evidence) that one of ordinary skill in the herbicidal art would have been motivated to make the modification of the prior art salts necessary to arrive at" the claimed invention.). Even a determination that it would have been obvious to one of ordinary skill in the art at the time of the invention to try the proposed modification or combination is not sufficient to establish a *prima facie* case of obviousness. *See In re Fine*, 837 F.2d 1071, 1075, 5 U.S.P.Q.2d 1596, 1599 (Fed. Cir. 1988).

In addition, the M.P.E.P. and the Federal Circuit repeatedly warn against using an Appellants' disclosure as a blueprint to reconstruct the claimed invention. For example, the M.P.E.P. states, "The tendency to resort to 'hindsight' based upon applicant's disclosure is often difficult to avoid due to the very nature of the examination process. However, impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art." M.P.E.P. § 2142. The governing Federal Circuit cases are equally clear. "A critical step in analyzing the patentability of claims pursuant to [35 U.S.C. § 103] is casting the mind back to the time of invention, to consider the thinking of one of ordinary skill in the art, guided only by the prior art references and the then-accepted wisdom in the field. . . . Close adherence to this methodology is especially important in cases where the very ease with which the invention can be understood may prompt one 'to fall victim to the insidious effect of a hindsight syndrome wherein that which only the invention taught is used against its teacher.'" *In re Kotzab,* 217 F.3d 1365, 1369, 55 U.S.P.Q.2d 1313, 1316 (Fed. Cir. 2000) (citations omitted). In *In re Kotzab*, the Federal Circuit noted that to prevent the use of hindsight based on the invention to defeat patentability of the invention, the court requires the Examiner to show a motivation to combine the references that create the case of obviousness. *See id. See also, e.g., Grain Processing Corp. v. American Maize-Products,* 840 F.2d 902, 907, 5 U.S.P.Q.2d 1788, 1792 (Fed. Cir. 1988). Similarly, in *In re Dembiczak*, the Federal Circuit reversed a finding of obviousness by the Board, explaining that the required evidence of such a teaching,

suggestion, or motivation is essential to avoid impermissible hindsight reconstruction of an applicant's invention:

> Our case law makes clear that the best defense against the subtle but powerful attraction of hind-sight obviousness analysis is *rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references*. Combining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability—the essence of hindsight.

175 F.3d at 999, 50 U.S.P.Q.2d at 1617 (emphasis added) (citations omitted).

B. The *Erreygers*, *Liu*, and *Fisher* References

In general, *Erreygers* discloses a repeater that "provides an efficient way to implement ADSL over long distances." (*Erreygers*, Abstract). The repeater unit includes high pass filters 56, 58, low pass filters 52, 54, and an ADSL repeater 60, which includes ADSL transceivers 62, 64. (*Id.*, Figure 2). *Erreygers*'s ADSL transceiver 62 "receives ADSL signals from high pass filter 56, amplifies the received ADSL signals, and sends the amplified ADSL signals to ADSL transceiver 64 for forwarding to high pass filter 58." (*Id.*, col. 5, ll. 42-59). The composition of *Erreygers* repeater unit 50 is shown in *Erreygers*, Figure 2.

Liu generally teaches an ADSL transceiver that is able to scale down a data transmission rate in a DMT modulated ADSL channel. (*Liu*, Abstract; *id.*, col. 2, ll. 62-65). *Liu*'s transceiver can separately scale the transmit rate and the receive rate. (*Id.*, col. 3, ll. 29-37). *Liu* focuses on the fact that signal processing capability requirements are reduced by a factor M (*Id.*, col. 6, ll. 41-43) -- "Based on a scaling factor M negotiated between transceiver 200 and an upstream transceiver, DMT Receiver Core 260 will only process one out of every M received blocks of DMT symbols." (*Id.*, col. 6, ll. 36-40). *Liu* includes circuitry for receiving an ADSL signal (*e.g.*, Filter and Analog/Digital Converter 280, Buffer 270, and Receiver Core 260) and circuitry for sending an ADSL signal (*e.g.*, DAC 230, Buffer 240, and DMT Tx Core 250). (*Id.*, Figure 2; *id.* at col. 5, l. 65 - col. 7, l. 28).

In *Liu*'s receiving branch, a received signal is filtered, sampled, and buffered by Filter and Analog/Digital Converter 280 and Buffer 270. (*Id.*, col. 6, ll. 17-26). The signal is then

passed to DMT Receiver Core 260, which "is responsible for extracting the original data stream." (*Id.*, col. 6, ll. 34-36). Independently, in *Liu*'s transmitting branch, the ADSL transceiver transmits a signal using the DAC 230 and buffer 240 of the front end transmitting circuit, which can have a different scaling factor than the receiving circuit. (*Id.*, col. 7, ll. 5-8). "[S]ymbols are generated by DMT Tx Core 250, [and] they are stored in Buffer 240 and then converted to analog wave forms by DAC 230." (*Id.*, col. 7, ll. 18-21). *Liu*'s separate receiving and transmitting branches are connected by the Control and Application Interface 245, which "permits the system to behave essentially like a conventional analog modem." (*Id.*, Figure 2; *id.*, col. 8, ll. 13-16).

Fisher generally teaches a data transmission system that sends a pilot tone with transmitted data. (*Fisher*, col. 1, ll. 36-47). The pilot tone allows a receiver clock to adjust so as to maintain synchronization between the sender and the receiver. (*Id.*, col. 1, ll. 47-56).

C. The *McGhee* Reference

The *McGhee* reference lists Cisco Technology, Inc. as the assignee, and Cisco Technology, Inc. is the assignee of the present Application. On information and belief, at the time the claimed invention was made, both the inventors of the *McGhee* reference and the inventors of the present Applications were under an obligation to assign their respective inventions to Cisco Technology, Inc. Finally, the *McGhee* reference, with an issue date of December 2, 2003, after the effective filing date of the present Application, would not qualify as prior art under 35 U.S.C. § 102 (a) or (b).

Thus, the *McGhee* reference is not available as prior art under 35 U.S.C. § 103. *See* 35 U.S.C. § 103 (c)(1) ("Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the claimed invention was made, owned by the same person or subject to an obligation of assignment to the same person."). Accordingly, Appellants have not discussed the teachings of the *McGhee* reference.

D. The proposed combinations fail to disclose, teach, or suggest each and every limitation of Appellants' Claims.

Appellants respectfully submit that *Erreygers*, *Liu*, *McGhee*, and *Fisher*, whether taken alone or in combination, fail to teach or suggest every element of Appellants' claims.

Consider, for example, independent Claim 1,[3] which recites:

> A method for providing greater reach of a DSL signal comprising:
> receiving an incoming DSL signal including a data signal;
> demodulating the data signal;
> requantizing the demodulated data signal by determining a constellation associated with each bit of data in the modulated data signal and resetting the value of that bit to the value of the constellation to acquire underlying data in the data signal and transform the data signal into a regenerated form;
> modulating the requantized data signal;
> amplifying the modulated requantized data signal; and
> transmitting the amplified signal in a regenerated form.

Among other aspects, the references, whether taken alone or in any combination, fail to teach or suggest: (1) "requantizing the demodulated data signal" and "modulating the requantized data signal," and (2) "requantizing the demodulated data signal by determining a constellation associated with each bit of data in the modulated data signal and resetting the value of that bit to the value of the constellation and transform the data signal into a regenerated form."

1. The references fail to teach or suggest both "requantizing the demodulated data signal" and "modulating the requantized data signal," as required by Claim 1.

First, Appellants respectfully submit that the references, whether taken alone or in combination, fail to teach or suggest "requantizing the demodulated data signal" and "modulating the requantized data signal," as required by Claim 1. As teaching these claimed aspects, the Examiner relies on the proposed *Erreygers-Liu* combination. (*Final Office Action*, pages 2-4). While the Examiner acknowledges that *Erreygers* does not disclose "transceivers perform[ing] demodulating, requantizing, modulating, and [] amplifying," the Examiner relies on a combination of *Erreygers* and *Liu* to teach both "requantizing the demodulated data signal" and "modulating the requantized data signal." (*Id.*)

[3] The Examiner rejects Claim 1 as unpatentable over the proposed *Erreygers-Liu* combination.

As discussed above, *Erreygers* discloses an ADSL repeater 60 that includes ADSL transceivers 62, 64. (*Erreygers*, Figure 2). *Erreygers*'s ADSL transceiver 62 receives, amplifies, and then transmits ADSL signals. (*Id.*, col. 5, ll. 42-59). While *Erreygers* may teach a repeater for implementing ADSL over long distances, *Erreygers* does not teach or suggest either "requantizing the demodulated data signal" or "modulating the requantized data signal," as required by Claim 1.

Liu also fails to teach or suggest these claimed aspects. As also discussed above, *Liu* includes circuitry for receiving an ADSL signal (*e.g.*, Filter and Analog/Digital Converter 280, Buffer 270, and Receiver Core 260) and circuitry for sending an ADSL signal (*e.g.*, DAC 230, Buffer 240, and DMT Tx Core 250). (*Liu*, Figure 2; *id.* at col. 5, l. 65 - col. 7, l. 28). *Liu*'s receiving branch and *Liu*'s transmitting branch are connected by the Control and Application Interface 245, which receives system configuration information from a host and identifies the data rate scaling factor (M). (*Id.*, Figure 2; *id.*, col. 6, ll. 55-62).

In the receiving branch, a received signal is filtered, sampled, and buffered by Filter and Analog/Digital Converter 280 and Buffer 270. (*Id.*, col. 6, ll. 17-26). The signal is then passed to DMT Receiver Core 260, which extracts the original data stream. (*Id.*, col. 6, ll. 34-36). Independently, in the transmitting branch, the ADSL transceiver transmits a signal after DMT Tx Core 250 generates symbols, Buffer 240 stores the symbols, and DAC 230 coverts the symbols to analog wave forms. (*Id.*, col. 7, ll. 5-8; *id.*, col. 7, ll. 18-21).

However, *Liu* fails to teach or suggest both "requantizing the demodulated data signal" and "modulating **the** requantized data signal," as required by Claim 1. (emphasis added). Even if one assumes, for the sake of argument, that *Liu* discloses: (a) in the receiving branch, requantizing the demodulated data signal and (b) in the transmitting branch, modulating outbound symbols, then *Liu* still fails to teach or suggest all aspects of Applicants' Claim 1 -- *Liu* fails to teach, suggest, or even mention that a data signal is demodulated and requantized (*e.g.*, in the receiving branch) and then, that same requantized data signal is modulated (*e.g.*, in the transmitting branch).

Accordingly, Appellants respectfully submit that *Liu* fails to teach or suggest both "requantizing the demodulated data signal" and "modulating the requantized data signal," as required by Claim 1. *Erreygers*, which does not teach or suggest either "requantizing the demodulated data signal" or "modulating the requantized data signal," fails to remedy the deficiencies of *Liu*.

Independent Claims 11, 16, 18, and 19 include limitations that, for substantially similar reasons, are not taught by the references, whether taken alone or in any combination. Accordingly, these independent Claims 1, 11, 16, 18, and 19, and their respective dependent claims, are not rendered obvious by the references.

For at least these reasons, Appellants respectfully submit that the rejection of Claims 1-3, 5-12, 14, and 16-26 is improper and should be reversed by the Board.

2. The references fail to teach or suggest the specific aspects required by Appellants' "requantizing ..." step in Claim 1.

The references also fail to disclose "requantizing the demodulated data signal by determining a constellation associated with each bit of data in the modulated data signal and resetting the value of that bit to the value of the constellation and transform the data signal into a regenerated form," as required by Claim 1. As disclosing Appellants' step of "requantizing," the Examiner relies solely on *Liu*.[4] (*Final Office Action*, pages 2-4).

As teaching these claimed aspects, the Examiner relies on *Liu*'s ADC 280 and DMT Core 260, stating:

> The received data is requantized first by ADC 280 (Fig.2), then demodulated by DMT core 260. The act of demodulating the signal comprises the step of requantizing the data to recover original data stream 201 (the original data is demodulated by comparing the received signal to a true value constellation, removing the carrier signals and making a judgment with each received data bit to the known true value constellation, then using the judgment to assign the recognized original data bit into another true value constellation where the original data stream is communicated to the rest of the system, for example, if the signaling is in binary, the data bits will be assigned (requantized) to either a '1' or a '0'.

(*Final Office Action*, p. 3). Appellants respectfully disagree. With regard to *Liu*'s ADC 280, *Liu* simply states:

> The full bandwidth signal is bandpass limited to a frequency width B by suitable, well-known techniques as it passes through bandpass Filter and Analog/Digital Converter 280. The received DMT signal is sampled (using any of a number of well-known techniques) and buffered in Buffer 270, which, in a preferred embodiment, is a FIFO.

(*Liu*, col. 6, ll. 17-22). With regard to *Liu*'s DMT Core 260, *Liu* merely states:

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[4] *See Final Office Action*, page 2 ("Erreygers does not specify that the transceivers perform demodulating, requantizing, modulating, and then amplifying the data signal.")

> . . . Buffer 270 stores only one DMT symbol from every set of M symbols received. That is, of the M symbols, M-1 symbols are not stored but simply discarded. This scales down the processing load of Receiver Core 260 by a factor of M.
>
> DMT Receiver Core 260 is responsible for extracting the original data stream from the numerous sub-carriers within any specific received DMT symbol block. Based on a scaling factor M negotiated between transceiver 200 and an upstream transceiver, DMT Receiver Core 260 will only process one out of every M received blocks of DMT symbols. The remaining M-1 frames are ignored or dropped as depicted visually in Figure 2.
>
> * * *
>
> DMT Rx core 260 is basically implemented the same way as specified by T1.413, but with some important differences, including the fact that it is only necessary to process one of every M DMT symbol blocks within the standard xDSL time period, the speed of FFT implementation can be slower and more cost-effective.

(*Id.*, col. 6, ll. 29-41 (emphasis added); *id.*, col. 8, ll. 7-12). There is no further disclosure in *Liu* of the operations of DMT Receiver Core 260, and certainly no disclosure of "requantizing the demodulated data signal by determining a constellation associated with each bit of data in the modulated data signal and resetting the value of that bit to the value of the constellation and transform the data signal into a regenerated form" by the DMT Receiver Core 260, as proposed by the Examiner.

Liu's disclosure that the "received DMT signal is sampled . . . and buffered" and that the "DMT Receiver Core 260 is responsible for extracting the original data steam" fails to teach or suggest, expressly or inherently, the specific aspects recited in Appellants' claim. Even assuming, for the sake of argument, that *Liu*'s devices could be modified to incorporate these specific aspects, *Liu* still fails to actually disclose, teach, or even suggest required aspects of Appellants' claims, *e.g.*, "requantizing the demodulated data signal by determining a constellation associated with each bit of data in the modulated data signal and resetting the value of that bit to the value of the constellation." (Claim 1; emphasis added). There is simply no disclosure in *Liu* of the specific aspects required by Claim 1. By maintaining the rejection of Claim 1 over the proposed *Erreygers-Liu* combination, the Examiner has read details into the references that simply are not there.

Accordingly, Appellants respectfully submit that *Liu* fails to teach or suggest Appellant's step of requantizing, as required by Claim 1. *Erreygers* fails to remedy the deficiencies of *Liu*.

Independent Claims 11, 16, 18, and 19 include limitations that, for substantially similar reasons, are not taught by the references, whether taken alone or in combination. Accordingly, these independent Claims 1, 11, 16, 18, and 19, and their respective dependent claims, are not rendered obvious by the references.

For at least these reasons, Appellants respectfully submit that the rejection of Claims 1-3, 5-12, 14, and 16-26 is improper and should be reversed by the Board.

3. At Least Dependent Claims 2, 7, 8, and 18-25 include separately patentable limitations.

The Examiner rejects Claims 2, 7, 8, and 18-25 as unpatentable over the proposed *Erreygers-Liu-McGhee* combination. With respect to each of these claims, the Examiner has relied upon *McGhee* specifically for disclosure of certain elements. For example, with respect to Claim 2, the Examiner relies upon *McGhee* for disclosure of "wherein the incoming DSL signal further includes a voice signal." As another example, the Examiner relies upon *McGhee* for disclosure of "wherein and further comprising combining the voice signal and the amplified data signal," as recited in Claim 7. As a further example, with respect to Claim 8, the Examiner relies upon *McGhee* for the disclosure of "further comprising filtering the voice signal into a first frequency range of approximately zero to four kilohertz and filtering the data signal into a second frequency range of approximately 25 kilohertz to 1.1. megahertz."

As Appellants have noted above in sub-section I.C., *McGhee* is not an available reference under Section 103. *See* 35 U.S.C. § 103 (c)(1). Since *Erreygers* and *Liu*, whether considered alone or in combination, do not disclose the elements recited in Appellants' Claims 2, 7, 8, and 18-25, Appellants submit that the rejections of Claims 2, 7, 8 and 18-25 under the proposed *Erreygers-Liu-McGhee* combination are improper.

For at least these reasons, Appellants respectfully submit that the rejections of Claims 2, 7, 8 and 18-25 should be reversed by the Board.

4. At Least Dependent Claims 3, 5, 22, and 23 include separately patentable limitations.

The Examiner rejects Claims 3 and 5 as unpatentable over the proposed *Erreygers-Liu* combination and rejects Claims 22 and 23 as unpatentable over the proposed *Erreygers-*

Liu-McGhee combination. (*Final Office Action*, pages 4-5 & 7). As Appellants have noted above in sub-section I.C, *McGhee* is not an available reference under Section 103. *See* 35 U.S.C. § 103 (c)(1). Accordingly, Appellants explain why dependent Claims 3, 5, 22, and 23 are not taught or suggested by the proposed *Erreygers-Liu* combination.

The proposed *Erreygers-Liu* combination fails to disclose "a Fast Fourier Transformer," as required by dependent Claims 3 and 22, and "an inverse Fast Fourier Transformer," as required by dependent Claims 5 and 23. Consider, for example, dependent Claim 3, which recites:

> The method of Claim 1, wherein demodulating the data signal comprises:
>
> converting the data signal from analog to digital form;
>
> dividing, by a Fast Fourier Transformer, the data signal in digital form into a plurality of desired data bins specified by frequency; and
>
> discarding data outside the plurality of desired data bins.

As teaching the claimed "Fast Fourier Transformer," the Examiner cites *Liu*, column 6, lines 1-10 and 34-54 and column 8, lines 1-10. (*Final Office Action*, page 4). However, *Liu* only once even arguably mentions a Fast Fourier Transformer, inverse Fast Fourier Transformer, FFT, or the like -- that portion of *Liu* states:

> (i) unlike hardware architectures implementing a full T1.413 ADSL standard, the present invention loads a DMT block in the receive Buffer 270 every M DMT symbols, where M is agreed to during a handshaking procedure between the upstream and downstream transceivers;
>
> (ii) DMT Rx core 260 is basically implemented the same way as specified by T1.413, but with some important differences, including the fact that it is only necessary to process one of every M DMT symbol blocks within the standard xDSL time period, <u>the speed of FFT implementation can be slower and more cost-effective</u>;

(*Liu*, col. 8, ll. 1-12 (emphasis added)). Even assuming, for the sake of argument, that this disclosure teaches a Fast Fourier Transformer, *Liu* fails to teach or suggest the elements specifically recited by Appellants claims.

For example, Claim 3 requires "dividing, by a Fast Fourier Transformer, the data signal in digital form into a plurality of desired data bins specified by frequency." As another example, Claim 5 requires "combining, by an inverse Fast Fourier Transformer, a plurality of requantized data in a plurality of data bins specified by frequency into a data signal in the time domain." As further example, Claim 22 requires "the first conditioning circuit comprises on analog-to-digital converter and a Fast Fourier Transformer for

demodulating the first data signal." As another example, Claim 23 requires "the first conditioning circuit comprises a digital-to-analog converter and an Inverse Fast Fourier Transformer for converting the first data signal into digital format."

For at least these reasons, Appellants respectfully submit that the rejections of Claims 3, 5, 22, and 23 are improper and should be reversed by the Board.

E. One of Ordinary Skill in the Art Would not have been Motivated to Make the Proposed Combinations

Appellants submit that the Examiner has not demonstrated the requisite teaching, suggestion, or motivation in *Erreygers*, *Liu*, *McGhee*, *Fisher*, or the knowledge generally available to those of ordinary skill in the art at the time of the invention to modify or combine *Erreygers*, *Liu*, *McGhee*, *Fisher* in the various manners the Examiner proposes. Additionally, Appellants submit that one of ordinary skill in the art at the time of the invention would not have been motivated to make the proposed combination. The rejections are improper and should be reversed for at least this additional reason.

As discussed above in sub-section I.A of this Appeal Brief, the question raised under 35 U.S.C. § 103 is whether the prior art taken as a whole would suggest the claimed invention taken as a whole to one of ordinary skill in the art at the time of the invention. Accordingly, even if all elements of a claim are disclosed in various prior art references, which is certainly not the case here as discussed above, the claimed invention taken as a whole cannot be said to be obvious without some reason given in the prior art why one of ordinary skill at the time of the invention would have been prompted to modify the teachings of a reference or combine the teachings of multiple references to arrive at the claimed invention. It is clear based at least on the many distinctions discussed above that the various proposed combinations of the references do not, taken as a whole, suggest the claimed invention, taken as a whole. Rather, Appellants respectfully submit that the Examiner has merely pieced together disjointed portions of references, with the benefit of hindsight using Appellants' claims as a blueprint, in an attempt to reconstruct Appellants' claims.

Rather than citing any evidence of a teaching, suggestion, or motivation to combine or modify the teachings of the references, the Examiner merely states that the teachings of

one reference would improve the teachings of another reference. With regard to independent Claim 1, for example, the Examiner states:

> It would have been obvious to one of ordinary skill in the art at the time of this application to utilize Liu's transceiver for each of the transceivers in series disclosed by Erreygers for the purpose of implementing flexible and scaleable transceivers in the receiver that may have greater compatibility with various types of ADSL transceivers at either the CPE side or central office side of the network.

(*Final Office Action*, page 4).

Applicants respectfully submit that this statement does not provide the required evidence of a teaching, suggestion, or motivation to combine or modify the references. This statement represents the subjective belief of the Examiner, does not point to any known authority, and therefore is not based on objective evidence of record. In response to Appellants' arguments, the Examiner argues:

> [E]xaminer contends that providing more flexible transceivers (the adaptive data rate transceiver taught by Liu) in the ADSL repeater taught by Erreygers (as mentioned in the previous office action) is a valid motivation to combine the references.

(*Final Office Action*, page 10). The *Final Office Action* makes similar arguments in response to the lack of motivation to combine *Liu* and *Erreygers* with *McGhee* and *Fisher*. (*Id.*) While the *Final Office Action* has essentially stated that the motivation is provided because the teachings of one reference may improve the teachings of another reference, the *Final Office Action* fails to point to any evidence sufficient to show a *prima facie* case of obviousness.

Prevailing Federal Circuit law and the M.P.E.P. set forth a strict legal standard for combining references. According to the M.P.E.P., "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." M.P.E.P. § 2143.01 (emphasis in original). "Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art" at the time of the invention. *Id.* The Examiner, however, fails to identify this required evidence.

According to the Federal Circuit, "a showing of a suggestion, teaching, or motivation . . . is an 'essential component of an obviousness holding.'" *Brown & Williamson Tobacco Corp. v. Philip Morris Inc.*, 229 F.3d 1120, 1124-25 (Fed. Cir. 2000) (quoting *C.R. Bard, Inc., v. M3 Systems, Inc.*, 157 F.3d 1340, 1352 (Fed. Cir. 1998)). Furthermore, while "evidence of a suggestion, teaching, or motivation . . . may flow from the prior art references themselves, the knowledge of one of ordinary skill in the art, or, in some cases, the nature of the problem to be solved, ... [t]he range of sources available . . . does not diminish the requirement for actual evidence." *In re Dembiczak*, 175 F.3d 994, 999 (Fed. Cir. 1999) (emphasis added). Thus, it is a factual question that cannot be resolved on subjective belief and unknown authority, but must be based on objective evidence of record. *See In re Lee*, 277 F.3d 1338, 1343-44 (Fed. Cir. 2002).

Accordingly, Appellants respectfully submit that the proposed *Erreygers-Liu*, *Erreygers-Liu-McGhee*, *Erreygers-Liu-Fisher*, and *Erreygers-Liu-McGhee-Fisher* combinations are improper and should not be used here to reject Appellants' claims.

For at least these reasons, Appellants respectfully submit that the rejection of Claims 1-3, 5-12, 14, and 16-26 is improper and should be reversed by the Board.

CONCLUSION

Appellants have demonstrated that the present invention as claimed in Claims 1-3, 5-12, 14, and 16-26 is patentably distinct from the cited art. Accordingly, Appellants respectfully request that the Board reverse the final rejection and instruct the Examiner to enter the proposed amendments and issue a Notice of Allowance of Claims 1-3, 5-12, 14, and 16-26.

The Commissioner is hereby authorized to charge the statutory fee of $500.00 for this Appeal Brief to Deposit Account No. 02-0384 of Baker Botts LLP. Although no other fees are believed due, the Commissioner is hereby authorized to charge any fees or credit any overpayment to Deposit Account No. 02-0384 of Baker Botts LLP.

Respectfully submitted,

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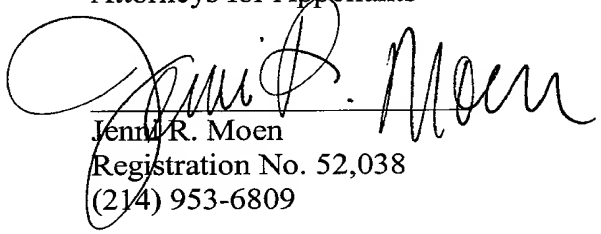

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Date: December 12, 2006

Customer No. **05073**

Claims Appendix

1. **(Previously Presented)** A method for providing greater reach of a DSL signal comprising:

receiving an incoming DSL signal including a data signal;

demodulating the data signal;

requantizing the demodulated data signal by determining a constellation associated with each bit of data in the modulated data signal and resetting the value of that bit to the value of the constellation to acquire underlying data in the data signal and transform the data signal into a regenerated form;

modulating the requantized data signal;

amplifying the modulated requantized data signal; and

transmitting the amplified signal.

2. **(Original)** The method of Claim 1, wherein the incoming DSL signal further includes a voice signal.

3. **(Original)** The method of Claim 1, wherein demodulating the data signal comprises:

converting the data signal from analog to digital form;

dividing, by a Fast Fourier Transformer, the data signal in digital form into a plurality of desired data bins specified by frequency; and

discarding data outside the plurality of desired data bins.

4. **(Canceled)**

5. **(Original)** The method of Claim 1, wherein modulating the requantized data signal comprises combining, by an inverse Fast Fourier Transformer, a plurality of requantized data in a plurality of data bins specified by frequency into a digital signal in the time domain and converting the digital signal in the time domain to an analog signal.

6. **(Original)** The method of Claim 1, wherein requantizing the demodulated data signal comprises requantizing the demodulated data signal in the frequency domain.

7. **(Original)** The method of Claim 2, wherein and further comprising combining the voice signal and the amplified data signal.

8. **(Previously Presented)** The method of Claim 2, further comprising filtering the voice signal into a first frequency range of approximately zero to four kilohertz and filtering the data signal into a second frequency range of approximately 25 kilohertz to 1.1 megahertz.

9. **(Original)** The method of Claim 1, wherein receiving the incoming DSL signal comprises receiving, by a resistive hybrid bridge, the incoming DSL signal.

10. **(Previously Presented)** The method of Claim 1, wherein transmitting the combined signal comprises transmitting, by a balanced bridge, the combined signal.

11. **(Previously Presented)** A method for providing greater reach of a DSL signal having a data portion, comprising:

demodulating the data portion;

requantizing the demodulated data portion by determining a constellation associated with each bit of data in the modulated data portion and resetting the value of that bit to the value of the constellation to acquire underlying data in the data portion and transform the data portion into a regenerated form;

modulating the requantized data portion;

amplifying the modulated requantized data portion; and

transmitting the amplified modulated requantized data portion.

12. **(Original)** The method of Claim 11, wherein demodulating the data portion comprises:

converting the data portion from analog to digital form;

dividing the data signal in digital form into a plurality of desired bins specified by frequency range; and

discarding data outside the plurality of desired bins.

13. **(Canceled)**

14. **(Original)** The method of Claim 11, wherein modulating the requantized data portion comprises combining a plurality of requanitized portions in a plurality of data bins specified by frequency into a digital signal in the time domain and converting the digital signal in the time domain to an analog signal.

15. **(Canceled)**

16. **(Previously Presented)** A system for facilitating greater reach of a DSL signal having a data portion, comprising:

a means for demodulating the data portion;

a means for requantizing the demodulated data portion by determining a constellation associated with each bit of data in the modulated data portion and resetting the value of that bit to the value of the constellation and transform the data portion into a regenerated form;

a means for modulating the requantized data portion; and

a means for amplifying the modulated requantized data portion.

17. **(Original)** The system of Claim 16, and further comprising a means for transmitting the amplified modulated requantized data portion.

18. **(Previously Presented)** A system for facilitating providing greater reach of a DSL signal comprising:

a means for splitting the DSL signal into separate voice and data signals;

a means for demodulating the data signal;

a means for requantizing the demodulated data signal by determining a constellation associated with each bit of data in the modulated data signal and resetting the value of that bit to the value of the constellation and transform the data signal into a regenerated form;

a means for modulating the requantized data signal; and

a means for combining and amplifying the voice and data signals into a combined signal.

19. **(Previously Presented)** A bi-directional DSL repeater and amplifier comprising:

a first signal detector operable to receive a first incoming DSL signal including a first data signal and direct the first incoming DSL signal to a first conditioning circuit and also operable to receive a first outgoing data signal from a second conditioning circuit and direct the first outgoing data signal over a first telephone line;

the first conditioning circuit being operable to:

receive a signal indicative of the first incoming DSL signal;

demodulate, requantize, and remodulate the first data signal to produce a first remodulated data signal, the first data signal requantized by determining a constellation associated with each bit of data in the modulated first data signal and resetting the value of that bit to the value of the constellation to acquire underlying data in the first data signal and transform the first data signal into a regenerated form; and

amplify the first remodulated data signal to produce a second outgoing data signal;

the second conditioning circuit being operable to:

receive a signal indicative of a second incoming DSL signal including a second data signal;

demodulate, requantize, and remodulate the second data signal to produce a second remodulated data signal, the second data signal requantized by determining a constellation associated with each bit of data in the modulated data signal and resetting the value of that bit to the value of the constellation to acquire underlying data in the second data signal and transform the second data signal into a regenerated form; and

amplify the second remodulated data signal to produce the first outgoing data signal; and

a second signal detector operable to receive the second incoming DSL signal and direct the second incoming DSL signal to the second conditioning circuit and also operable to receive the second outgoing data signal from the first conditioning circuit and direct the second outgoing data signal over a second telephone line.

20. **(Original)** The bi-directional DSL repeater and amplifier of Claim 19 wherein the first conditioning circuit comprises a low band filter and a high band filter for filtering the incoming DSL signal into a voice and the first data signal.

21. **(Original)** The bi-directional DSL repeater and amplifier of Claim 19, wherein the first conditioning circuit comprises a requantizer for requantizing the first data signal.

22. **(Original)** The bi-directional DSL repeater and amplifier of Claim 19, wherein the first conditioning circuit comprises on analog-to-digital converter and a Fast Fourier Transformer for demodulating the first data signal.

23. **(Original)** The bi-directional DSL repeater and amplifier of Claim 19, wherein the first conditioning circuit comprises a digital-to-analog converter and an Inverse Fast Fourier Transformer for converting the first data signal into digital format.

24. **(Original)** The bi-directional DSL repeater and a amplifier of Claim 19, wherein the first conditioning circuit comprises a data acquirer and re-transmitter for demodulating, requantizing, and remodulating the first data signal.

25. **(Original)** The bi-directional DSL repeater and amplifier of Claim 20, wherein the first conditioning circuit comprises a first amplifier for amplifying the first voice signal and a second amplifier for amplifying the first remodulated data signal.

26. **(Original)** The bi-directional DSL repeater and amplifier of Claim 19, wherein the first signal detector comprises a resistive hybrid bridge.

Evidence Appendix 1

Erreygers

US006236664B1

(12) **United States Patent**
Erreygers

(10) **Patent No.: US 6,236,664 B1**
(45) **Date of Patent: May 22, 2001**

(54) **PAIR GAIN SYSTEM WITH AN ADSL REPEATER UNIT**

(75) Inventor: **Jan Erreygers**, Tielt-Winge (BE)

(73) Assignee: **Terayon Communications Systems, Inc.**, Santa Clara, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/326,768**

(22) Filed: **Jun. 4, 1999**

(51) **Int. Cl.**[7] **H04L 12/28**
(52) **U.S. Cl.** **370/492**; 370/352; 370/356
(58) **Field of Search** 370/492, 392, 370/241, 540, 535, 477, 246, 274, 501, 356, 352, 353; 375/215; 348/6; 379/90.01, 93.01, 338–379

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European Telecommunications Standards Institute (ETSI) Specification No. TS 101 388 V1.1.1 (1998–11), "Coexistence of ADSL and ISDN–BA on the Same Pair" (1998–11) (referred to and incorporated by reference at page 7, lines 24–26, of this application).

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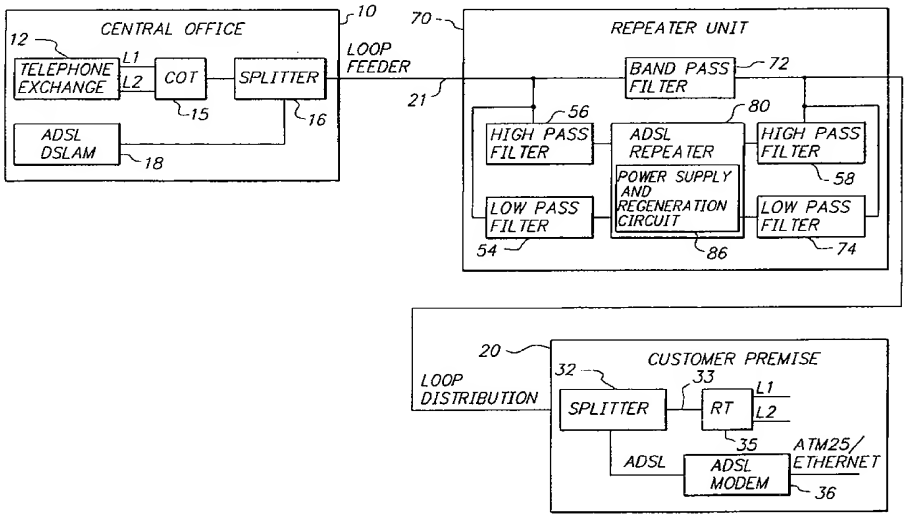
Primary Examiner—Wellington Chin
Assistant Examiner—Prenell Jones

(57) **ABSTRACT**

The present invention provides an efficient way to implement ADSL over long distances by combining a repeater for ADSL with a pair gain system, whereby the pair gain system remotely provides DC power to the repeater over the same pair as that for transmission of DSL and ADSL signals. The invention allows telecom operators to save huge costs in implementing ADSL over long distances, without sacrificing the quality of signal transmission. According to an embodiment of the invention, a telecommunication system comprises a central office system, a customer premise system and a repeater unit. The central office system provides and receives digital subscriber line (DSL) and asymmetrical DSL (ADSL) signals over a first pair of wires. The central office system also provides DC power to the repeater unit via the first pair. The customer premise system receives and sends DSL and ADSL signals over a second pair of wires. The repeater unit is coupled between the first and second pairs of wires for receiving an ADSL signal from the central office system via the first pair and providing a repeated ADSL signal to the customer premise system via the second pair. The repeater unit also receives an ADSL signal from the customer premise system via the second pair and provides a repeated ADSL signal to the central office system via the first pair.

20 Claims, 4 Drawing Sheets



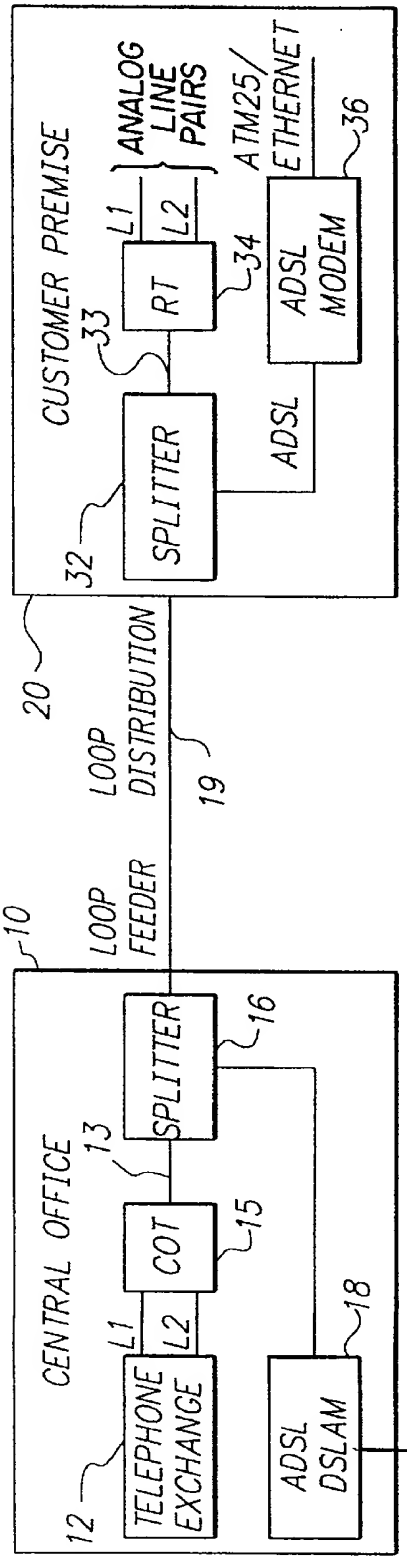


FIG. 1
(PRIOR ART)

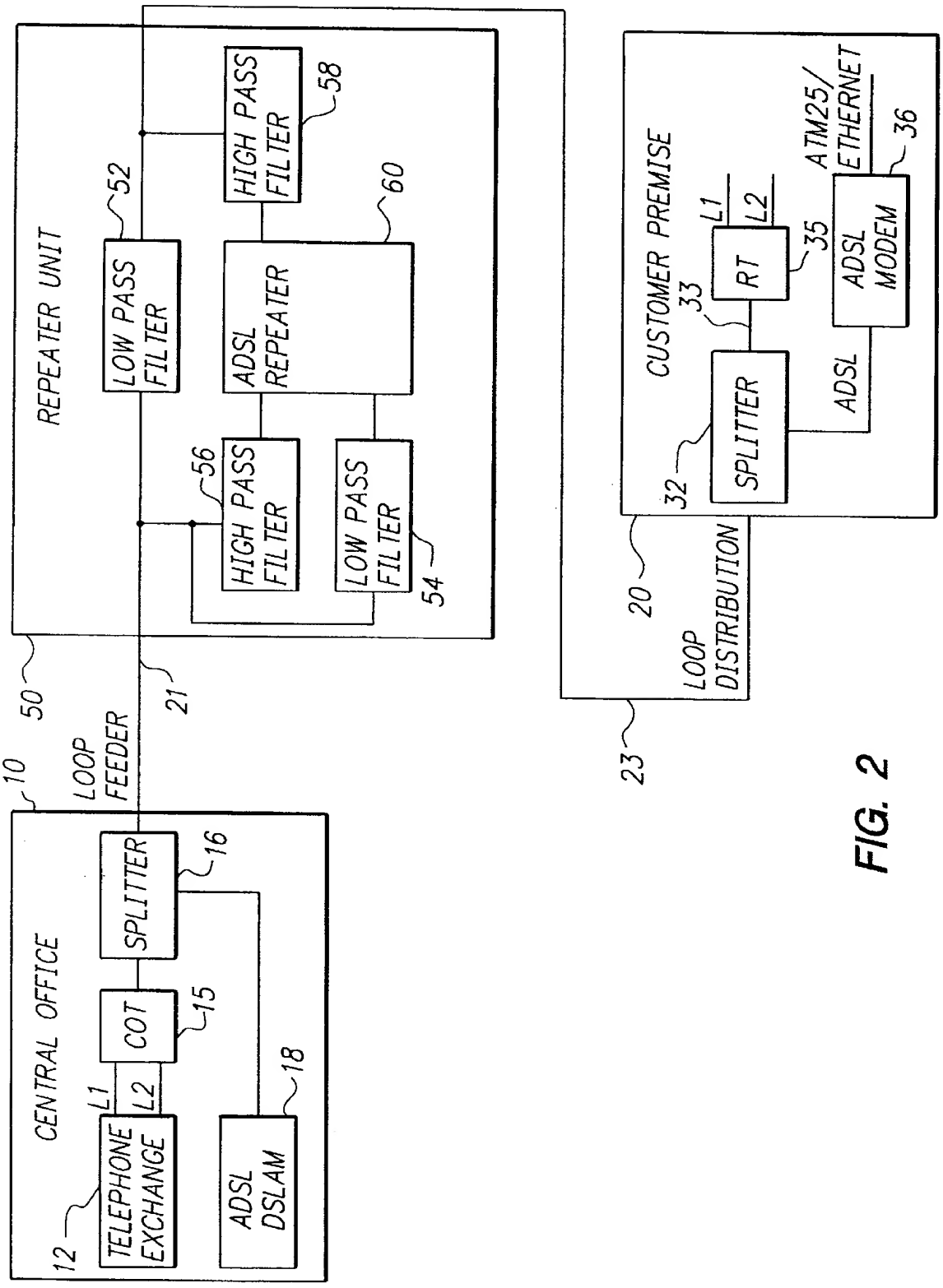

REPEATER UNIT
LOW PASS FILTER
52
HIGH PASS FILTER
58
ADSL REPEATER
60
HIGH PASS FILTER
56
LOW PASS FILTER
54
50
21
LOOP FEEDER
10
CENTRAL OFFICE
SPLITTER
16
COT
15
L1
L2
TELEPHONE EXCHANGE
12
ADSL DSLAM
18
CUSTOMER PREMISE
33
RT
35
L1
L2
ATM25/ ETHERNET
36
ADSL MODEM
ADSL
SPLITTER
32
20
LOOP DISTRIBUTION
23

FIG. 2

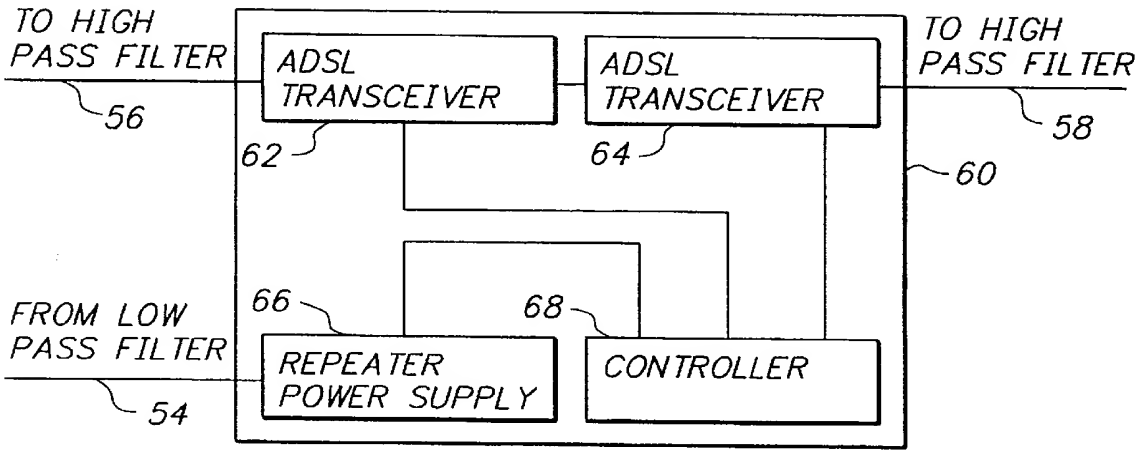

TO HIGH PASS FILTER
56
ADSL TRANSCEIVER
62
ADSL TRANSCEIVER
64
TO HIGH PASS FILTER
58
60
FROM LOW PASS FILTER
54
66
REPEATER POWER SUPPLY
68
CONTROLLER

FIG. 3

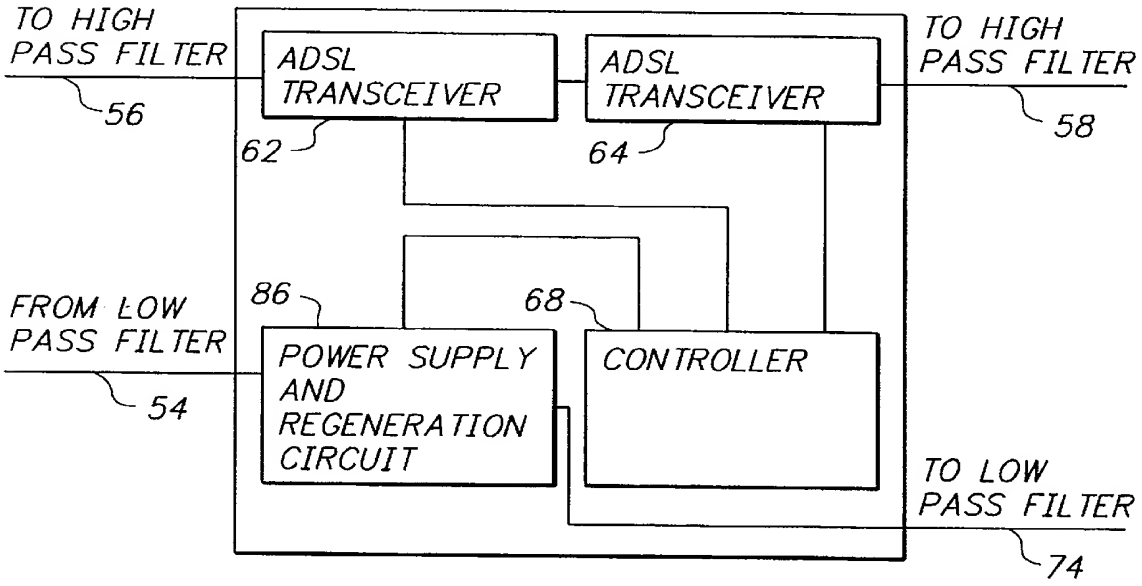

TO HIGH PASS FILTER
56
ADSL TRANSCEIVER
62
ADSL TRANSCEIVER
64
TO HIGH PASS FILTER
58
FROM LOW PASS FILTER
54
86
POWER SUPPLY AND REGENERATION CIRCUIT
68
CONTROLLER
TO LOW PASS FILTER
74

FIG. 5

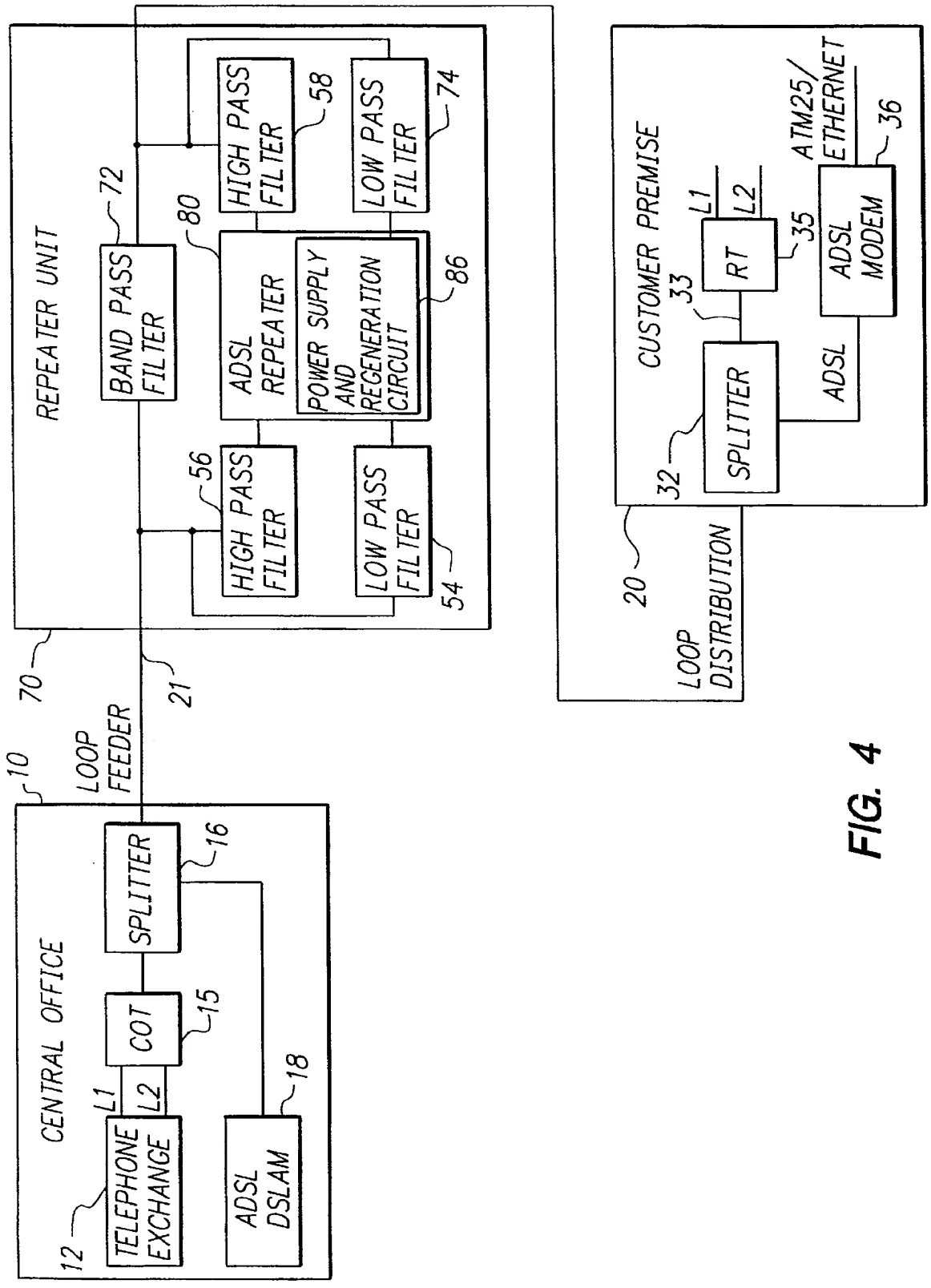

CENTRAL OFFICE
10
TELEPHONE EXCHANGE
12
L1
L2
COT
15
SPLITTER
16
ADSL DSLAM
18
LOOP FEEDER
21
REPEATER UNIT
70
BAND PASS FILTER
72
80
HIGH PASS FILTER
56
LOW PASS FILTER
54
ADSL REPEATER
POWER SUPPLY AND REGENERATION CIRCUIT
86
HIGH PASS FILTER
58
LOW PASS FILTER
74
LOOP DISTRIBUTION
20
CUSTOMER PREMISE
32
SPLITTER
33
L1
L2
RT
35
ADSL
ADSL MODEM
ATM25/ ETHERNET
36

FIG. 4

PAIR GAIN SYSTEM WITH AN ADSL REPEATER UNIT

BACKGROUND OF THE INVENTION

The invention relates generally to telecommunication systems, and more particularly to ADSL (Asymmetrical Digital Subscriber Line) transmission systems in access network.

Telephone customers are moving in an evolutionary way to higher bandwidths, from sharing POTS (Plain Old Telephone Service) and modem on one line to dedicated analog modem line at 56 kbps (kilo-bits per second) and to ISDN BA (Basic Access). Now, ADSL has been introduced and become proven technology. ADSL refers to a high-speed transmission technology using existing twisted pair of wires that permits simultaneous POTS and high-speed data communication. Generally, a higher data rate is employed downstream than upstream. Ordinary twisted pair equipped with ADSL modems can transmit movies, television, dense graphics, and very high speed data. For all its capacity, ADSL leaves POTS undisturbed. A single ADSL line therefore offers simultaneous channels for personal computers, televisions, and telephones. With ADSL, telephone companies can connect homes and businesses to exciting new interactive broadband services.

The ADSL services are different from ISDN services. ISDN provides two 64 kbps channels for voice or data, while ADSL is predominantly a data pipe providing an asymmetrical bandwidth of up to 9 Mbps downstream and 800 kbps upstream. The customers for ADSL most likely already have a dedicated modem line or ISDN.

FIG. **1** shows a conventional way of implementing ADSL over a pair gain system. A pair gain system is a system which typically includes a central office terminal (COT) located in a central office (CO) of a telephone company and a remote terminal (RT) located in a customer premises. The COT may have two or more line cards, each for connecting to a pair of wires from a telephone exchange in the CO. The COT of a pair gain system multiplexes signals received from the multiple pairs connected to its line cards, over a single pair connecting between the COT and the RT of the pair gain system. The COT also demultiplexes signals received from the RT via the single pair and provides them to the telephone exchange via the multiple pairs connected to its line cards. The RT demultiplexes signals received from the single pair and provides them to a subscriber at the customer premises over the same number of pairs. The RT also multiplexes signals received from the multiple pairs at the customer premises, over the single pair connecting to the COT. Thus, a pair gain system allows a subscriber at the customer premises to have two or more telephone lines without requiring the expense of installing additional pairs between the CO and the customer premises. An example of a pair gain system is the Miniplex® 2N1, which multiplexes two pairs over a single pair. Miniplex® 2N1 is commercially available from Raychem Corporation, Menlo Park, Calif.

As illustrated in FIG. **1**, at a CO **10** of a telephone company, a telephone exchange **12** provides two analog POTS lines L1 and L2 in the form of two twisted pairs of wires to a COT **15** of a pair gain system. COT **15** multiplexes L1 and L2 over a single twisted pair **13** and converts the analog signals from L1 and L2 into DSL (Digital Subscriber Line) signals, such as ISDN signals, on pair **13**. An ADSL DSLAM (DSL Access Multiplexer) **18** receives broadband data from the Internet, for example and provides high-speed data transmission in the form of ADSL signals. The DSL and

ADSL signals provided respectively from COT **15** and ADSL DSLAM **18** are fed to splitter **16**. Splitter **16** combines the DSL and ADSL signals for transmission to a customer premises **20** over a single twisted pair **19**. Splitter **16** also receives the DSL signals and ADSL signals from splitter **32** and separates the DSL signal from the ADSL signal for transmission to COT **15** and ADSL DSLAM **18**, respectively.

At customer premises **20**, splitter **32** separates the DSL signal from the ADSL signal. The DSL signal is provided, via a pair **33**, to a RT **34** of the pair gain system, which demultiplexes the DSL signal into analog signals on two analog POTS lines L1 and L2. Each of lines L1 and L2 at customer premises **20** is for connecting to a telecommunication device (not shown), such as a telephone or a fax machine. The ADSL signal is provided to an ADSL modem **36**, which is connected to either ATM **25** (asynchronous transfer mode 25 Mbps) or Ethernet. RT **34** also multiplexes analog signals from analog lines L1 and L2 into a DSL signal over pair **33** for transmission to CO **10**. Splitter **32** also receives DSL and ADSL signals from RT **34** and ADSL modem **36** respectively, and combines them for transmission to CO **10** over twisted pair **19**. In the case of implementing ADSL over ISDN BA (basic access), an ISDN NT1 (network termination 1) can be used as RT **34**.

One of the main limitations of ADSL is the loop length which is the distance between the CO or DSLAM and the customer premises. For service with a downstream speed of 5 to 6 Mbps (mega-bits per second), the loop length is limited to less than 12 kft, in order not to sacrifice the transmission quality. At the present time, telecom operators use very conservative installation rules to ensure that the service will always be properly delivered. However, they will soon receive requests for service from people living farther away from the central office where a DSLAM is located. At present, it is estimated that about 60% of the subscribers can be potentially reached and receive high-speed data services. This leaves the other 40% with only low-speed data services.

Of course, there are several solutions for delivering high bandwidth services over longer distances (e.g. fiber optics). One solution is the use of a repeater for the ADSL signal. However, ADSL repeaters face a specific issue with power feeding as the ADSL signal is usually transmitted simultaneously with POTS on a copper pair. In order that a repeater be practical in the field, it will need to receive remote power feeding. This is very difficult and may be impossible if ADSL is implemented with POTS on the same copper pair.

An easy solution is to run POTS and ADSL on different pairs. Several POTS lines can be multiplexed over one copper pair using subscriber line multiplexers. The copper pair used for ADSL can carry a DC current for remote power feeding an ADSL repeater. However in this case telecom operators must install two copper pairs in order to provide one or more POTS lines and an ADSL. Therefore, substantial additional expenses will be incurred by telecom operators for installing a second copper pair whenever ADSL service is requested to be delivered over longer distances.

Accordingly, there is a need for implementing ADSL over POTS over longer distances without requiring an additional copper pair for transmitting an ADSL signal along with a DC current to a customer premises.

SUMMARY OF THE INVENTION

The present invention provides an efficient way to transmit ADSL and multiple POTS signals over long distances by

combining a repeater for ADSL with a pair gain system, whereby the pair gain system remotely provides DC power to the repeater over the same pair as that for transmission of DSL and ADSL signals.

According to one embodiment of the invention, a telecommunication system is provided. The telecommunication system comprises a first transmission/receiving system, located at a first location, that provides and receives a first type of signal in a first frequency spectrum and a second type of signal in a second frequency spectrum over a first pair of wires; a second transmission/receiving system, located at a second location, that receives and sends the first and second types of signals over a second pair of wires; and a repeater unit, coupled between the first and second pairs of wires, for receiving a second type of signal from the first transmission/receiving system via the first pair and providing a repeated second type of signal to the second transmission/receiving system via the second pair, the repeater unit also receiving a second type of signal from the second transmission/receiving system via the second pair and providing a repeated second type of signal to the first transmission/receiving system via the first pair; wherein the first transmission/receiving system provides DC power to the repeater unit via the first pair. In one example, the first type of signal is a digital subscriber line (DSL) signal and the second type of signal is an asymmetrical DSL (ADSL) signal. The first transmission/receiving system includes a central office system having a pair gain central office terminal (COT) that converts analog signals into a DSL signal. Also, the second transmission/receiving system includes a customer premises system having a pair gain remote terminal (RT) that converts a DSL signal into analog signals. Furthermore, the COT provides the DC power to the repeater unit via the first pair of wires. The repeater unit may also regenerate the DC power to a higher voltage level and provide regenerated (voltage-boosted) power to the RT over the second pair of wires.

In this embodiment of the invention, the repeater unit comprises an ADSL repeater including a power supply circuit, the ADSL repeater receiving an ADSL signal and providing a corresponding repeated ADSL signal; a first low pass filter, coupled between the first and second pairs of wires, for allowing only DSL and DC signals to pass through; a second low pass filter, coupled between the first pair of wires and the ADSL repeater, for allowing only a DC signal to pass through to the power supply circuit of the ADSL repeater; a first high pass filter, coupled between the first pair of wires and the ADSL repeater, for allowing only the ADSL signal to pass through; and a second high pass filter, coupled between the ADSL repeater and the second pair of wires, for allowing only the ADSL signal to pass through.

According to an alternative embodiment of the invention, the repeater unit comprises an ADSL repeater including a power supply and regeneration circuit that regenerates DC signals to predetermined higher voltage values, the ADSL repeater receiving an ADSL signal and providing a corresponding repeated ADSL signal; a band pass filter, coupled between the first and second pairs of wires, for allowing only a DSL signal to pass through; a first low pass filter, coupled between the first pair of wires and the ADSL repeater, for allowing only a DC signal to pass through to the power supply and regeneration circuit of the ADSL repeater; a second low pass filter coupled between the power supply and regeneration circuit of the ADSL repeater and the second pair of wires for allowing only a DC signal to pass through;

a first high pass filter, coupled between the first pair of wires and the ADSL repeater, for allowing only the ADSL signal to pass through; and a second high pass filter, coupled between the ADSL repeater and the second pair of wires, for allowing only the ADSL signal to pass through.

Accordingly, the present invention allows telecom operators to save huge costs in implementing ADSL over long distances, without sacrificing the quality of signal transmission.

Other objects and attainments together with a fuller understanding of the invention will become apparent and appreciated by referring to the following description and claims taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings wherein like reference symbols refer to like parts:

FIG. **1** shows a conventional way of implementing ADSL over a pair gain system;

FIG. **2** illustrates a functional block diagram of one embodiment of the present invention;

FIG. **3** illustrates a functional block diagram of an ADSL repeater of the embodiment in FIG. **2**;

FIG. **4** shows a functional block diagram of an alternative embodiment of the present invention; and

FIG. **5** illustrates a functional block diagram of an ADSL repeater of the alternative embodiment in FIG. **4**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. **2** shows a functional block diagram of one embodiment of the present invention. In this embodiment, ADSL signals are transmitted together with basic rate ISDN (ISDN-BA) signals, which is equivalent to the technology of 2B1Q at 160 kbps, such as used by 2N1 Miniplex®, commercially available from Raychem Corporation, Menlo Park, Calif. Typically, in the this embodiment the bit rate of ADSL signal transmission is reduced by 10% compared to an embodiment in which ADSL signals are transmitted over POTS. Implementation of ADSL over ISDN-BA is described in more detail in European Telecommunications Standards Institute (ESTI) specification TS 101 388 V1.1.1 (1998-11), the disclosure of which is hereby incorporated by reference.

As illustrated in FIG. **2**, a central office **10** provides ISDN and ADSL services to a customer premises **20** via a repeater unit **50**, which includes low pass filters **52** and **54**, high pass filters **56** and **58**, and an ADSL repeater **60**. Except for the pair gain system which includes a COT **15** and a RT **35**, the functional blocks shown in central office **10** and customer premises **20** represent the same conventional components as those described above in connection with FIG. **1**. Therefore, for simplicity the description of these components is omitted. COT **15** and RT **35** are also conventional ones, except that COT **15** uses a higher powering voltage and delivers more current and RT **35** receives a fraction of the current delivered from COT **15**. The power calculations for COT **15** and RT **35** will be described later.

In ADSL repeater unit **50** shown in FIG. **2**, low pass filter **52** preferably has a cutoff frequency of 100 kHz and is bi-directional. Low pass filter **52** is connected between central office **10** and customer premises **20** for filtering signals received over segments **21** and **23** of the twisted pair.

There are three signals on the twisted pair: the DC power feeding current with a frequency spectrum of 0 to 10 Hz, the pair gain DSL 2B1Q signal with a frequency spectrum of 1 to 80 kHz, and the ADSL signal with a frequency spectrum of 120 to 1000 kHz. Low pass filter **52** allows the DC current and the DSL signal to pass through, but blocks the ADSL signal. Low pass filter **52** needs to be bi-directional because the DSL signal is full duplex and the repeated downstream ADSL signal should not go back towards CO exchange **12**.

Low pass filter **54** of repeater unit **50** preferably has a cutoff frequency of 100 Hz. It is connected between central office **10** and ADSL repeater **60** for filtering the signals received from segment **21** of the twisted pair and provides a high impedance for the DSL and ADSL signals. Low pass filter **54** allows only the DC current to pass through to the power supply circuit of ADSL repeater **60**. This allows central office **10** to remotely provide DC power to repeater unit **50**. In FIG. **2**, low pass filter **54** is preferably a uni-directional filter.

High pass filter **56** of repeater unit **50** preferably has a cutoff frequency of 100 kHz and is connected between central office **10** and ADSL repeater **60**. High pass filter **56** blocks the DC current and the DSL signal and allows the ADSL signal to pass through to ADSL repeater **60**. High pass filter **58** of repeater unit **50** preferably has a cutoff frequency of 100 kHz and is connected between ADSL repeater **60** and customer premises **20**. High pass filter **58** allows the repeated ADSL signal from ADSL repeater **60** to pass through to customer premises **20**. High pass filter **58** also filters signals received from customer premises **20** and allows only the ADSL signal to pass through to ADSL repeater **60**. In FIG. **2**, high pass filters **56** and **58** are preferably bi-directional filters.

In FIG. **2**, ADSL repeater **60** receives the downstream signal from high pass filter **56** and remodulates it for transmission towards the subscriber at customer premises **20**. The subscriber at customer premises **20** would not recognize any difference from a standard ADSL over pair gain system. ADSL repeater **60** also receives the upstream signal from high pass filter **58** and remodulates it for transmission towards central office **10**.

FIG. **3** shows a functional block diagram of ADSL repeater **60**, which includes ADSL transceivers **62** and **64**, a repeater power supply **66** and a controller **68**. ADSL transceivers **62** and **64** are conventional devices. An example of such transceiver is CopperGold MC 145650 commercially available from Motorola, or TNETD 3000C commercially available from Texas Instruments. ADSL transceiver **62** receives ADSL signals from high pass filter **56**, amplifies the received ADSL signals, and then sends the amplified ADSL signals to ADSL transceiver **64** for forwarding to high pass filter **58**. Similarly, ADSL transceiver **64** receives ADSL signals from high pass filter **58**, amplifies the ADSL signals, and then sends the amplified ADSL signals to ADSL transceiver **62** for forwarding to high pass filter **56**. Low pass filter **54** provides DC signals to repeater power supply **66** for powering ADSL repeater **60**. Controller **68** controls the operations of ADSL transceivers **62** and **64**.

FIG. **4** shows an alternative embodiment of the present invention. For simplicity, description of the elements with the same reference symbols as those previously described is omitted. In this embodiment, the DSL signals received by repeater unit **70** pass through a bi-directional band pass filter **72** having a frequency spectrum preferably between 100 Hz and 100 kHz. Band pass filter **72** blocks the DC signals. The DC power feeding current supplied from central office **10** passes through low pass filter **54** to power ADSL repeater **80**. A power supply and regeneration circuit **86** in ADSL repeater **80** will regenerate the feeding voltage to a predetermined higher value for sending, via a low pass filter **74**, to customer premises to power RT **35**. Like low pass filter **54**, low pass filter **74** has a cutoff frequency of approximately 100 Hz. This embodiment allows signals to be transmitted over longer distances.

FIG. **5** shows a functional block diagram of ADSL repeater **80**, which, except for power supply and regeneration circuit **86**, is similar to ADSL repeater **60** shown in FIG. **3**. Therefore, detailed description of FIG. **5** is omitted.

The systems in FIGS. **2** and **4** each are shown for ADSL combined with a 2:1 pair gain system, i.e., 2 lines multiplexed over one pair. For example, one can use a Miniplex® 2N1 pair gain system commercially available from Raychem Corporation, Menlo Park, Calif. It is also possible to use a pair gain system with more than 2:1, e.g., a 4:1 pair gain system—4 lines multiplexed over one pair, such as a Miniplex® 4N1 pair gain system, which is also commercially available from Raychem Corporation. A 4:1 pair gain system uses more bandwidth, but the same principles apply. For an ADSL over a 4:1 pair gain system, the bit rate may be about 20% lower than for the full-rate of an ADSL over POTS. This is not so critical when the ADSL repeater unit of the present invention is used. If the full rate can achieve 6 Mbps over a loop length of 10,000 ft, then an ADSL over 4:1 pair gain system should be able to reach a speed of 5 Mbps. With the aid of an ADSL repeater unit of the present invention, a speed of 5 Mbps over a loop length of 20,000 ft can be achieved.

The power calculations for the pair gain system in FIG. **2** are now described. The known and unknown values in the calculations are listed below:

The known values are:

Prt: power consumption of the Miniplex® RT,

Prep: power consumption of the ADSL repeater,

Rf: resistance of the feeder part of the loop,

Rd: resistance of the distribution part of the loop, and

Vlc: powering voltage at the line card of the pair gain COT.

The unknown values are:

Vrt: voltage at the RT,

Irt: current drawn by the RT,

Vrep: voltage at the repeater,

Irep: current drawn by the repeater, and

Ilc: current to be delivered by the Miniplex® COT.

The following equations are used for power calculations for the pair gain system in FIG. **2**.

$$Prt=Vrt*Irt \quad (1)$$

$$Vrep=Vrt+Rd*Irt \quad (2)$$

$$Prep=Vrep*Irep \quad (3)$$

$$Vlc=Vrep+Rf*Ilc \quad (4)$$

$$Ilc=Irep+Irt \quad (5)$$

From (1) and (3):

$$Irt=Prt/Vrt \quad (6)$$

$$Irep=Prep/Vrep \quad (7)$$

By substituting equations (6) and (7) in equations (2) an (3), the following are derived:

$$Vrt=Vrep-Rd*(Prt/Vrt) \quad (8)$$

$$Vrep=Vlc-Rf*((Prep/Vrep)+(Prt/Vrt)) \quad (9)$$

It is easy to solve (8) and (9) together iteratively by using, e.g., a spreadsheet, such as Microsoft Excel®.

The following examples illustrate the power calculations for two different systems: ADSL over 2:1 pair gain system and ADSL over 4:1 pair gain system. In the calculations of the these examples, it is assumed that Miniplex® 2N1 and Miniplex® 4N1 pair gain systems are used. Furthermore, the following assumptions are made:

power consumption of an ADSL repeater unit=6 W,

power consumption of Miniplex® 2N1 RT=4 W,

power consumption of Miniplex® 4N1 RT=6 W.

Also, all the powering voltages and currents remain within the GR-1089 A3 limits, as provided by Bellcore, "Electromagnetic Compatibility and Electrical Safety—Generic Criteria for Network Telecommunications Equipment," Issue 2, December 1997. The results of the calculations are shown in Table 1.

TABLE 1

Comparison of various parameters in power calculations for different systems

	ADSL over Miniplex ® 2N1 pair gain system with ADSL repeater unit	ADSL over Miniplex ® 4N1 pair gain system with ADSL repeater unit
Prep	6 W	6 W
Prt	4 W	6 W
Rf	800 Ohm (resistance for a length of ± 10 kft)	800 Ohm (resistance for a length of ± 10 kft)
Rd	600 Ohm	400 Ohm
Vlc	200 V	250 V
Vrep	138 V	200 V
Vrt	118 V	188 V
Irt	34.0 mA	32 mA
Irep	43.4 mA	30 mA
Ilc	77.4 mA	62 mA

The power calculations for the pair gain system in FIG. **4** are next described.

The known values are:

Prt: power consumption of the Miniplex® RT,

Prep: power consumption of the ADSL repeater,

Rf: resistance of the feeder part of the loop,

Rd: resistance of the distribution part of the loop, and

Vlc: powering voltage at the line card of the pair gain COT.

Vrepout powering voltage at the output of the repeater

Eff_rep efficiency of the voltage boosting circuit in the repeater

The unknown values are:

Vrt: voltage at the RT,

Irt: current drawn by the RT,

Prepout power delivered from the repeater to the Miniplex® RT

Vrep: input voltage at the repeater,

Ilc: current to be delivered by the Miniplex COT.

The following equations are used for power calculations for the pair gain system in FIG. **4**.

$$Prt=Vrt*Irt \quad (10)$$

$$Vrepout=Vrt+Rd*Irt \quad (11)$$

$$Prepout=Vrepout*Irt \quad (12)$$

$$Prep+(Prepout/Eff\_rep)=Vrep*Ilc \quad (13)$$

$$Vlc=Vrep+Rf*Ilc \quad (14)$$

From (10) and (11):

$$Irt=Prt/(Vrepout-Rd*Irt) \quad (15)$$

This can be readily solved for Irt. Substituting the value of Irt in (12) provides the value for Prepout.

Combining (13) and (14) gives:

$$Ilc*(Vlc-Rf*Ilc)=Prep+(Prepout/Eff\_rep) \quad (16)$$

This can be readily solved for Ilc. Substituting the value of Ilc in (13) or (14) allows one to calculate the value of Vrep.

The following examples illustrate the power calculations for two different systems: ADSL over 2:1 pair gain system and ADSL over 4:1 pair gain system. In the calculations of the these examples, it is assumed that Miniplex® 2N1 and Miniplex® 4N1 pair gain systems are used. Furthermore, the following assumptions are made:

power consumption of an ADSL repeater unit=6 W,

power consumption of Miniplex® 2N1 RT=4 W,

power consumption of Miniplex® 4N1 RT=6 W.

Also, all the powering voltages and currents remain within the GR-1089 A3 limits, as provided by Bellcore, "Electromagnetic Compatibility and Electrical Safety—Generic Criteria for Network Telecommunications Equipment," Issue 2, December 1997. The results of the calculations are shown in Table 2.

TABLE 2

Comparison of various parameters in power calculations for different systems

	ADSL over Miniplex ® 2N1 pair gain system with ADSL repeater unit	ADSL over Miniplex ® 4N1 pair gain system with ADSL repeater unit
Prep	6 W	6 W
Prt	4 W	6 W
Rf	800 Ohm (resistance for a length of ± 10 kft)	800 Ohm (resistance for a length of ± 10 kft)
Rd	600 Ohm	400 Ohm
Vlc	200 V	250 V
Vrepout	200 V	250 V
Eff_rep	0.80	0.80
Vrep	142 V	201 V
Vrt	187 V	240 V
Irt	21.4 mA	25.0 mA
Ilc	72.3 mA	60.8 mA

While the invention has been described in conjunction with several specific embodiments, it is evident to those skilled in the art that many further alternatives, modifications and variations will be apparent in light of the foregoing description. For example, the invention could also be used in VDSL (Very-high-bit rate DSL) applications. Thus, the invention described herein is intended to embrace all such alternatives, modifications, applications and variations as may fall within the spirit and scope of the appended claims.

What is claimed is:

1. A telecommunications system including a twisted wire pair extending from a central office location to a subscriber premises location, the system comprising:

a digital subscriber line (DSL) transmission/receiving system connected to the twisted wire pair and having a

pair gain central office terminal (COT) located at the central office location, that converts a first plurality of analog telecommunications signals into a DSL signal and supplies the DSL signal and operating power over the twisted wire pair and having a pair gain remote terminal (RT) at the subscriber premises location that obtains the DSL signal and operating power from the twisted wire pair and converts the DSL signal into the first plurality of analog telecommunications signals;

an asymmetrical digital subscriber line (ADSL) transmission/receiving system connected to the twisted wire pair and having an ADSL access multiplexer located at the central office location, that bidirectionally translates central office broadband data into central office ADSL signals and subscriber ADSL signals into subscriber broadband data, and having an ADSL modem at the subscriber premises location that bidirectionally translates subscriber broadband data into subscriber ADSL signals and central office ADSL signals into central office broadband data; and

an ADSL repeater unit, coupled to the twisted wire pair, for selectively receiving and bidirectionally repeating the ADSL signals via the twisted wire pair, said ADSL repeater unit also receiving operating power from the DSL COT via the twisted wire pair;

wherein said ADSL repeater unit extends the useful length of the twisted wire pair for carrying the ADSL signals.

2. The telecommunications system set forth in claim **1** wherein the ADSL repeater unit includes a repeater power supply connected to the twisted wire pair for regenerating COT supplied operating power to a predetermined higher voltage value and for supplying the regenerated operating power over the twisted wire pair to operate the DSL RT.

3. The system of claim **1** wherein:

said central office location further includes a first splitter that receives a DSL signal from the COT and an ADSL signal from the ADSL access multiplexer, and provides a combined DSL signal to said customer premises location, and an ADSL signal to said ADSL repeater unit, via the twisted wire pair; and

the first splitter also receives combined a DSL signal and a repeated ADSL signal via the twisted wire pair, separates the DSL signal from the repeated ADSL signal, provides the DSL signal to the COT, and provides the repeated ADSL signal to the ADSL access multiplexer.

4. The system of claim **3** wherein:

said customer premise system further includes a second splitter that receives combined a DSL signal, and a repeated ADSL signal from said repeater unit, via the twisted wire pair, separates the DSL signal from the repeated ADSL signal, provides the DSL signal to the RT, and provides the repeated ADSL signal to the ADSL modem; and

the second splitter also receives a DSL signal from the RT and an ADSL signal from the ADSL modem and provides a combined DSL signal to the COT and an ADSL signal to said repeater unit via the twisted wire pair.

5. The system of claim **1** wherein the twisted wire pair comprises a first segment between said central office location and said ADSL repeater, and a second segment between said ADSL repeater and said subscriber premises location, and said ADSL repeater unit comprises:

a power supply circuit for drawing repeater operating power from the COT via the first segment,

a first low pass filter, coupled between the first and second segments, for allowing only DSL type signals and DC power signals to pass through;

a second low pass filter, coupled between the first segment and the ADSL repeater unit, for allowing only the DC power signal to pass through to the repeater power supply;

a first high pass filter, coupled between the first segment and the ADSL repeater, for allowing only the ADSL signal to pass through; and

a second high pass filter, coupled between the ADSL repeater and the second segment, for allowing only the ADSL signal to pass through.

6. The system of claim **5** wherein the ADSL repeater receives a downstream ADSL signal from said central office location and remodulates it to provide a corresponding repeated ADSL signal to said customer premises location, the ADSL repeater also receiving an upstream ADSL type signal from the customer premises location and remodulating it to provide a corresponding repeated ADSL type signal to said central office location.

7. The system of claim **5** wherein:

the first low pass filter has a cutoff frequency of approximately 100 kHz;

the second low pass filter has a cutoff frequency of approximately 100 Hz; and

the first and second high pass filters each have a cutoff frequency of approximately 100 kHz.

8. The system of claim **1** wherein the twisted wire pair comprises a first segment between said central office location and said ADSL repeater, and a second segment between said ADSL repeater and said subscriber premises location, and the ADSL repeater unit comprises:

a power supply and regeneration circuit that regenerates DC signals to predetermined higher values,

a band pass filter, coupled between the first and second segments, for allowing only a DSL signal to pass through;

a first low pass filter, coupled between the first segment and the ADSL repeater, for allowing only DC power to pass through to the repeater power supply and regeneration circuit;

a second low pass filter, coupled between the repeater power supply and the second segment for allowing only a regenerated DC power signal to pass through;

a first high pass filter, coupled between the first segment and the ADSL repeater, for allowing only the ADSL signal to pass through; and

a second high pass filter, coupled between the ADSL repeater and the second segment, for allowing only the ADSL signal to pass through.

9. The system of claim **8** wherein the ADSL repeater receives a downstream ADSL signal from said central office system and remodulates it to provide a corresponding repeated ADSL signal to said customer premises location, the ADSL repeater also receiving an upstream ADSL signal from the customer premises location and remodulating it to provide a corresponding repeated ADSL signal to said central office location.

10. The system of claim **8** wherein:

the band pass filter has a frequency band between approximately 100 Hz to 100 kHz;

the first and second low pass filter each have a cutoff frequency of approximately 100 Hz; and

the first and second high pass filters each have a cutoff frequency of 100 kHz.

11. A method for extending bandwidth and useful service distance of a twisted wire pair telecommunications service loop between a central office location and a subscriber premises location, comprising the steps of:

(a) providing and receiving digital subscriber line (DSL) signals and providing DSL remote terminal operating power with a DSL central office terminal (COT) at the central office location; and providing and receiving DSL signals and drawing operating power with a DSL remote terminal (RT) at the subscriber premises location, using the twisted wire pair;

(b) providing and receiving asymmetric DSL (ADSL) signals with a central office ADSL transmission/receiving unit at the central office location; and providing and receiving ADSL signals at an ADSL remote unit at the subscriber premises location, using the twisted wire pair;

(c) providing repeated ADSL signals within the telecommunications service loop with an ADSL repeater unit connected to the twisted wire pair at a location intermediately between the central office location and subscriber premises location; and

(d) providing operating power to the ADSL repeater unit from the DSL COT via the twisted wire pair.

12. The method of claim 11 wherein step (c) includes further steps of:

providing a power supply circuit within the ADSL repeater unit,

receiving an ADSL signal and providing a corresponding repeated ADSL with the ADSL repeater unit;

passing only DSL signals and operating power through a first low pass filter within the ADSL repeater unit, coupled to the twisted wire pair;

passing only operating power through a second low pass filter, coupled between the twisted wire pair and the repeater power supply circuit;

passing only ADSL signals through a first high pass filter, coupled between the twisted wire pair and the ADSL repeater unit; and

passing only ADSL signals through a second high pass filter coupled between the ADSL repeater and the twisted wire pair.

13. The method of claim 12 wherein step (c) includes:

receiving and remodulating a downstream ADSL signal from the central office ADSL transmitting/receiving unit to provide a corresponding repeated ADSL signal to the ADSL remote unit at the subscriber premises location, using the ADSL repeater and the twisted wire pair, and

receiving and remodulating an upstream ADSL signal from the ADSL remote unit at the subscriber premises location to provide a corresponding repeated ADSL type signal to the central office ADSL transmitting/receiving unit, using the ADSL repeater and the twisted wire pair.

14. The method of claim 12 wherein:

the first low pass filter has a cutoff frequency of 100 kHz;

the second low pass filter has a cutoff frequency of 100 Hz; and

the first and second high pass filters each have a cutoff frequency of 100 kHz.

15. The method of claim 11 wherein step (c) includes steps of:

providing a power supply and regeneration circuit that regenerates COT supplied operating power to predetermined higher voltage values;

receiving an ADSL signal and providing a corresponding repeated ADSL signal;

passing only DSL type signals through a band pass filter coupled to the twisted wire pair;

passing only operating power through a first low pass filter, coupled between the twisted wire pair and the ADSL repeater unit power supply such that only operating power passes through to the power supply and regeneration circuit of the ADSL repeater;

passing only regenerated operating power through a second low pass filter coupled between the repeater power supply and the twisted wire pair;

passing only ADSL signals through a first high pass filter coupled between a first segment of the twisted wire pair leading to the central office ADSL unit and the ADSL repeater unit; and

passing only ADSL signals through a second high pass filter coupled between the ADSL repeater unit and a second segment of the twisted wire pair leading to the subscriber premises ADSL unit.

16. The method of claim 15 wherein step (c) includes steps of:

receiving and remodulating a downstream ADSL signal from the central office ADSL transmission/receiving unit to provide a corresponding repeated ADSL signal to the ADSL remote unit at the subscriber premises location using the ADSL repeater and the second segment; and,

receiving and remodulating an upstream ADSL signal from the ADSL remote unit at the subscriber premises location and remodulating it to provide a corresponding repeated ADSL signal to the central office ADSL transmission/receiving unit, using the ADSL repeater unit and the first segment.

17. The method of claim 15 wherein:

the band pass filter has a frequency band between approximately 100 Hz to 100 kHz;

the first and second low pass filter each have a cutoff frequency of approximately 100 Hz; and

the first and second high pass filters each have a cutoff frequency of 100 kHz.

18. The method of claim 11 comprising the further step of regenerating COT supplied operating power to a predetermined higher voltage value with a power supply of the ADSL repeater unit and supplying regenerated operating power over the twisted wire pair to operate the DSL RT.

19. An asynchronous digital subscriber line (ASDL) service repeater unit for extending bandwidth and useful service distance of a twisted wire pair telecommunications service loop extending from a central office location to a subscriber premises location, the central office location including a first telecommunications system comprising a pair gain digital subscriber line (DSL) central office terminal (COT) for supplying DSL signals and operating power over the service loop and a DSL remote terminal (RT) connected to receive DSL signals and operating power at the subscriber premises location, and a second telecommunications system comprising a central office asynchronous DSL (ADSL) unit at the central office location for supplying ASDL signals over the service loop and a subscriber premises ADSL unit at the subscriber premises location for receiving ADSL signals via the service loop; the ADSL service repeater unit being connected to the service loop intermediately of the central office location and the subscriber premises location and including:

signal filtering means for passing the DSL signals without modification, and for separating the operating power and the ADSL signals,

a pair of ADSL transceivers for respectively repeating ADSL signals from the central office ADSL unit to the subscriber premises ADSL unit and from the subscriber premises ADSL unit to the central office ADSL unit, and

a repeater power supply for providing operating power for operating the pair of ADSL transceivers, and for regenerating the operating power to a predetermined higher voltage level and sending the regenerated operating power over the service loop to provide regenerated operating power for operating the DSL RT.

20. The ADSL service repeater unit set forth in claim **19** further comprising a repeater controller connected to control the pair of ADSL transceivers.

* * * * *

Evidence Appendix 2

Liu

US006088385A

United States Patent [19]

Liu

[11] Patent Number: 6,088,385

[45] Date of Patent: Jul. 11, 2000

[54] **FLEXIBLE AND SCALABLE RATE ADSL TRANSCEIVER AND SYSTEM**

[75] Inventor: **Ming-Kang Liu**, Cupertino, Calif.

[73] Assignee: **Integrated Telecom Express**, Santa Clara, Calif.

[21] Appl. No.: **09/026,030**

[22] Filed: **Feb. 19, 1998**

Related U.S. Application Data

[63] Continuation-in-part of application No. 08/884,895, Jun. 30, 1997, which is a continuation-in-part of application No. 08/884,956, Jun. 30, 1997, which is a continuation-in-part of application No. 08/884,957, Jun. 30, 1997, which is a continuation-in-part of application No. 08/884,958, Jun. 30, 1997, which is a continuation-in-part of application No. 08/884,959, Jun. 30, 1997, which is a continuation-in-part of application No. 08/884,979, Jun. 30, 1997.

[51] **Int. Cl.**[7] **H04B 1/38**; H04L 5/16

[52] **U.S. Cl.** **375/219**; 375/372

[58] **Field of Search** 375/219, 220, 375/225, 259, 260, 372, 371; 370/412, 493–495

[56] **References Cited**

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Primary Examiner—Chi H. Pham

Assistant Examiner—Jean B. Corrielus

Attorney, Agent, or Firm—Law &

[57] **ABSTRACT**

A high speed modem is described that implements a scalable data rate ADSL link. The target data rate of the modem is scaled appropriately relative to a maximum available protocol rate by a factor M based on the signal processing capabilities available for performing DMT modulation and demodulation. An upstream transceiver is informed of the proposed scaling factor during a handshaking procedure, and thereafter the data rate of the channel is then scaled down by sending M copies of the same DMT symbol to the upstream transceiver, which effectively reduces the rate by such factor M. A self-executing calibration routine can be used for determining the appropriate scaling factor for such device, or alternatively, in some contexts a user can configure such scaling factor directly through a suitable interface. The invention can be implemented as a stand-alone unit with a self-contained DSP for performing necessary signal processing, or as a software modem located within a personal computer or similar computing device including portable digital devices such as cell phones, personal digital assistants, etc.

65 Claims, 2 Drawing Sheets

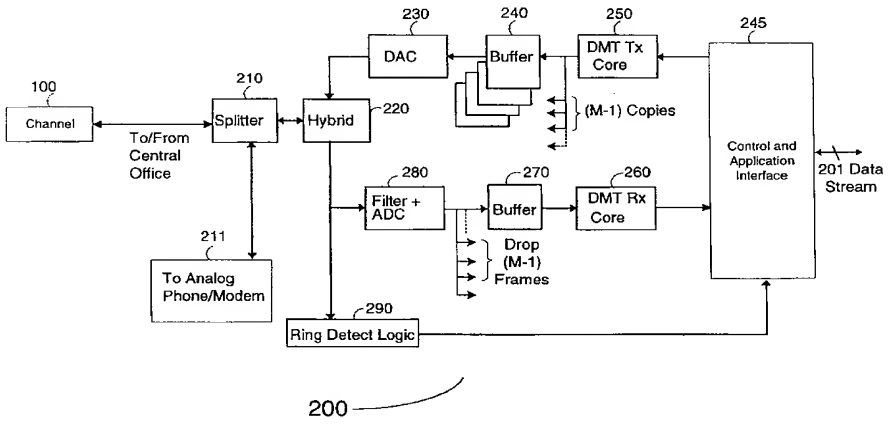


FIGURE 1

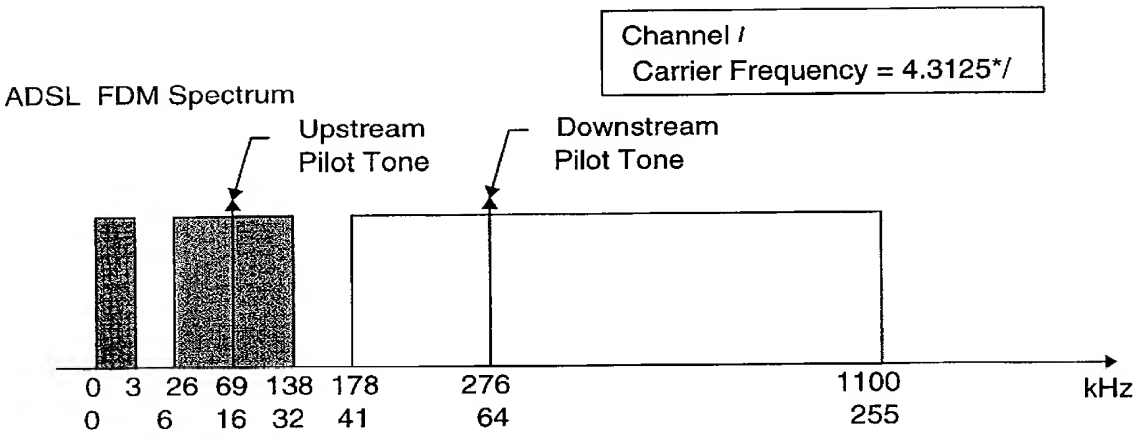
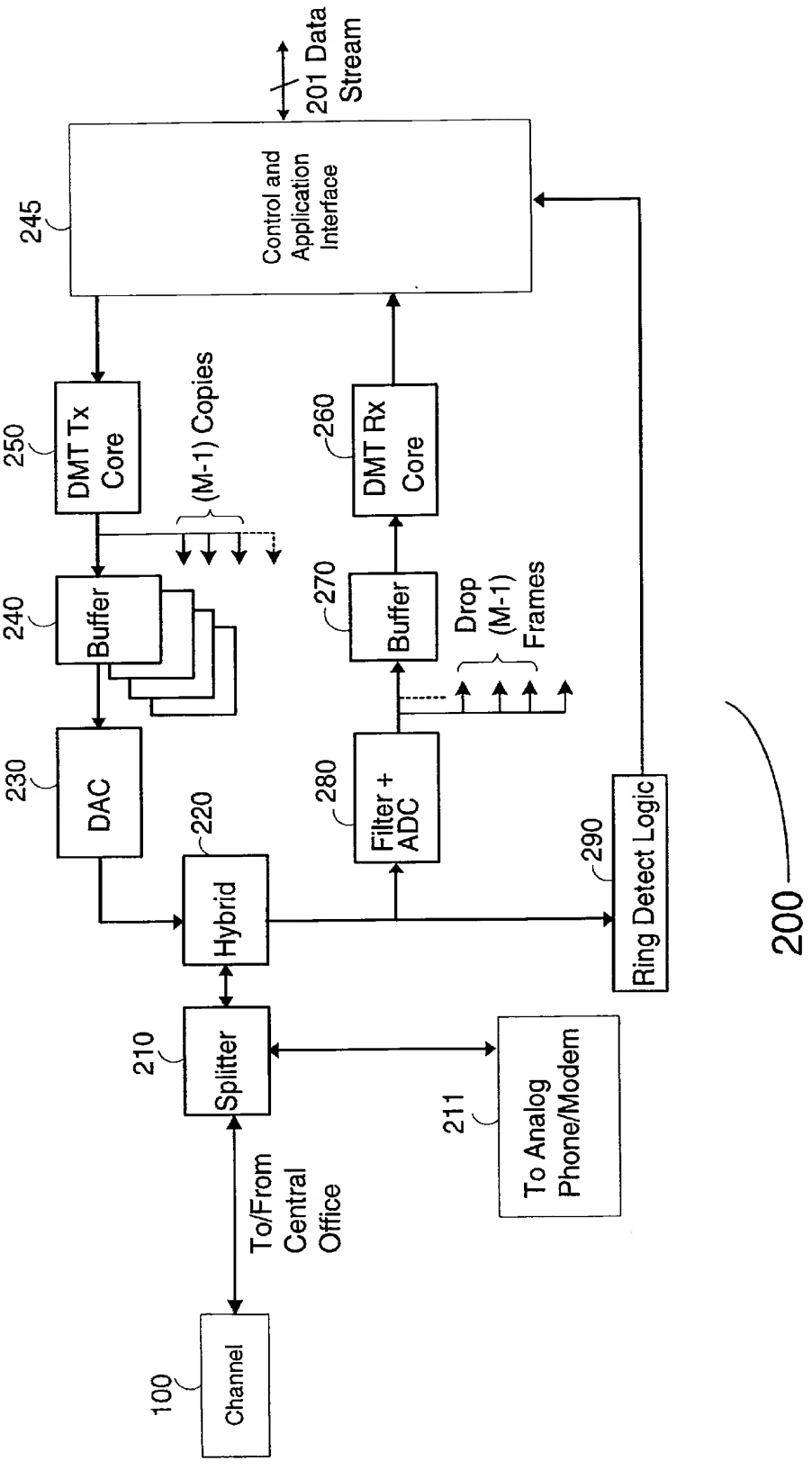

Channel *I*
Carrier Frequency = 4.3125*/
ADSL FDM Spectrum
Upstream
Pilot Tone
Downstream
Pilot Tone
0 3 26 69 138 178 276 1100
0 6 16 32 41 64 255
kHz

FIGURE 2


201 Data Stream
Control and Application Interface
245
DMT Tx Core
250
(M-1) Copies
DMT Rx Core
260
Buffer
240
Buffer
270
Drop (M-1) Frames
DAC
230
Filter + ADC
280
Hybrid
220
Ring Detect Logic
290
200
Splitter
210
To Analog Phone/Modem
211
To/From Central Office
Channel
100

FLEXIBLE AND SCALABLE RATE ADSL TRANSCEIVER AND SYSTEM

CROSS REFERENCE TO RELATED APPLICATIONS

The present application is a continuation-in-part of the following additional applications:

- Ser. No. 08/884,895, filed Jun. 30, 1997 for a "Forward Compatible And Expandable High Speed Communications System & Method of Operation";
- Ser. No. 08/884,956, filed Jun. 30, 1997 for a "Device Driver For Rate Adaptable Modem With Forward Compatible and Expandable Functionality";
- Ser. No. 08/884,957, filed Jun. 30, 1997 for "Software Rate Adaptable Modem with Forward Compatible and Expandable Functionality & Method of Operation";
- Ser. No. 08/884,958, filed Jun. 30, 1997 for "Modular Multiplicative Data Rate Modem & Method of Operation";
- Ser. No. 08/884,959, filed Jun. 30, 1997 for a "User Controllable Applications Program For Rate Adaptable Modem With Forward Compatible and Expandable Functionality."
- Ser. No. 08/884,979, filed Jun. 30, 1997 for a "Rate Adaptable Modem With Forward Compatible and Expandable Functionality & Method of Operation."

The above applications are hereby expressly incorporated by reference.

FIELD OF THE INVENTION

The invention relates generally to an improved high-speed communications system that establishes a data link using only a selectable and scalable portion of the total available bandwidth (potential downstream data transmission) of a channel. In particular, the present invention permits the characteristics (including target data rate) of an ADSL link to be controlled based on the capabilities of the processing power of a host system that is responsible for implementing a software modem. The system is scalable in performance based on the available signal processing power of such processor, and permits a user to increase throughput to the point of achieving full potential of the available channel bandwidth.

BACKGROUND OF THE INVENTION

In the prior applications noted above, it was pointed out that Asymmetric Digital Subscriber Line (ADSL) is becoming more and more and popular for high-speed modem applications. The ANSI T1.413 ADSL standard uses a technology called Discrete Multi-Tone (DMT) that sends data over 255 separate frequency channels, and each 4 kHz frequency channel can be made to provide a bit rate up to the best present day voice band (33.6 kb/s) modems. This results essentially in overall performance that is equivalent to around two hundred V0.34 modems used in parallel on the same line. Because each channel can be configured to a different bit rate according to the channel characteristics, it can be seen that DMT is inherently "rate-adaptive" and extremely flexible for interfacing with different subscriber equipment and line conditions.

A number of problems arise, however, in attempting to implement a full scale ADSL transceiver cost-effectively, especially in a software modem environment where available signal processing power can vary significantly and unpredictably from device to device. For example, a state of the art desktop computer using the latest microprocessor technology may have a potential signal processing capability many times higher than a simple hand-held computing device. The processor within such devices must also tend to a number of additional operating system and application tasks which limits the available computational time for processing DMT received/transmit symbols. Moreover, DMT technology requires advanced analog front end (AFE) devices that can also push current technology limits and imposes both high cost and power consumption. Both of these facts make a full-scale ADSL implementation undesirable for new and contemplated classes of hand-held personal computing devices. Furthermore, requiring a communications device (such as a modem) to fully support the total throughput of a standard such as ADSL may be unnecessary when prospective users of high-speed data links do not need to use all the available bandwidth provided by such standards.

As disclosed in the above prior applications, an ADSL implementation that permits users to throttle or scale the data throughput in a manner they can control, based on their particular application needs, hardware cost budget, etc., is far more efficient and desirable. As such, one approach discussed at length in the above applications for controlling data bandwidth or throughput is to initiate a link in which the transmitting spectrum of the ADSL signal is confined to a particular set of frequencies (or sub-channels) so that the overall data rate can be restricted to a range suitable for the user setting up the channel. By informing an upstream transceiver that only a selected set of sub-channels should be used, and controlling this sub-set, a user can also thereafter scalably increase the data rate through suitable hardware adjustments, including by adding additional AFE stages that permit a larger section of the ADSL signal to be processed. In this manner, the data rate is scaled by processing a larger and larger portion of a regular ADSL signal within a given ADSL symbol period.

The merits of a scalable data rate ADSL transceiver, therefore, are well known. Nevertheless, the above solution may not be optimal for all possible environments, in the sense that it may not be the simplest, most cost-effective, most flexible, etc. It would also be extremely desirable if it were possible to reduce the effective data rate in other controllable ways which are flexible, easily implementable within the ADSL protocol, and which optimize computational loading on available signal processing circuitry. For example, in an ADSL software modem context, it would be extremely useful if the receive and transmit data rates could be controlled entirely by software updates and modifications, rather than by hardware changes. To date, however, this capability does not exist in prior art ADSL modems.

SUMMARY OF THE INVENTION

An object of the present invention therefore is to provide a communications system which is fully compatible with high speed, rate adaptable modulation protocols such as used with ADSL, but which system is nevertheless implementable with simpler digital signal processing circuitry and is thus reduced in cost and complexity;

Another objective of the present invention is to provide a method for scaling down a data transmission rate in a DMT modulated ADSL channel by processing only a limited number of symbols in a DMT signal;

Another objective of the present invention is to provide a high speed communications system having a data through-

put that is easily and finely controllable and expandable through software control, so that the performance range of such system can be configured to any fractional percentage of total bandwidth available in a transmission channel, up to and including full bandwidth use of the channel;

These objects and others are accomplished by providing a scalable data rate transceiver which includes a channel interface circuit for receiving an analog data signal from an upstream transceiver through a conventional digital subscriber loop channel. The upstream transceiver negotiates with the transceiver on the value of a data rate scaling factor M. Thereafter, the upstream transceiver transmits M identical copies of an analog data signal, which is sampled by a front end receiving circuit and converted into M identical digital signals. In a preferred embodiment, the analog data signals are DMT symbols representing a number of modulated sub-channels of an ADSL signal. A data buffer is coupled to the front end receiving circuit and is loaded with one of the copies of the M signals. A signal processing circuit (either a dedicated DSP or a host processor accessible to the data buffer through a data channel) then need only process one of the M identical digital signals, which results in a controlled, scaled data rate reduction by such factor M. In a preferred embodiment, therefore, a maximum xDSL data rate R available in a digital subscriber loop is scaled to a rate R/M to reduce computational load and processing requirements of a signal processor used in the signal processing circuit.

In another embodiment, a separate upstream transmit data rate R' is also scaled by a factor M' as well, resulting in a scaled data rate R'/M' and thus providing yet another measure of control over the computation load on a signal processing circuit. The values of M and M' can be independently controlled so as to effectuate a maximum transmit rate, a maximum receive rate, a minimum amount of data computational load on the signal processing circuit, etc. Such values for M and M' are generally based on signal processing capabilities available to the transceiver and can be determined by a calibration routine or determined by a user of a host processing device based on system parameter options presented to the user by an applications program running on the host processing device.

The present invention can be implemented either with a standalone dedicated signal processor in a conventional hardware modem configuration, or, alternatively, as a software modem utilizing the native processing capability of a host processing device for signal processing requirements. In a software modem embodiment, a bus interface circuit is needed for transmitting the digital signals from the data buffer to a host processing device, and for receiving a transmission control signal from the host processing device to cause the upstream transmitter to transmit at a data rate substantially equal to the scaled data rate R/M.

Although the inventions are described below in a preferred embodiment implementing the ADSL standard, it will be apparent to those skilled in the art the present invention would be beneficially used in any high speed rate-adaptable applications.

It should be noted that while some prior art devices also have limited mechanisms for achieving a reduction of nominal or peak transmission speed in a channel, they only activate or implement such mechanisms as a fallback response to a failure in the channel, or because of a transmission rate reduction in the upstream transceiver. Unlike the present invention, such prior art modems, during an initialization process, attempt to establish the highest possible transmission rate achievable by the channel and the upstream transceiver. In other words, any rate reduction imposed by the downstream modem is typically considered an unintended and undesirable side effect of bad channel characteristics and not a desirable and intentional design target as set forth in the present invention. In addition, the data rate reduction in such modems is accomplished primarily by varying the number of bits per baud (hertz) at a fixed frequency, and not by controlling the number of symbols that can be provided in a downstream data transmission.

Similarly, while a fixed 300 baud rate downstream modem can work with an upstream 33 kb/s rate modem this arrangement is also unlike the present invention. This is because, again, the bandwidth reduction in such prior art device is so large that it is considered commercially unusable by today's standards. Furthermore, the smaller bandwidth modem is not compatible with, and does not support, the higher protocols of the higher bandwidth modem, which is also undesirable from an implementation standpoint. Stated another way, unlike the present invention, the lower end modem limitations of prior art system force the data link to be set up using a low level protocol that does not take advantage of the full capabilities of more advanced protocols.

Finally, there is no mechanism for users of either of the prior art systems noted above to expand the functionality of such modems in a controlled, flexible, and modular manner.

The present invention therefore further builds on and complements the approach of our earlier-filed channel rate control applications. In particular, the present invention performs a time domain scaling (rather than a frequency domain scaling) of the ADSL signal in order to scale down the available channel data rate. The computational load of an ADSL system employing the present invention can be scaled by negotiating a scaling factor M with the remote transceiver, based on the processing power available in (or to) the user transceiver. By virtue of the fact that software control (rather than fixed hardware performance constraints) is utilized to configure the scaling factor M, more granular control over the channel data rate can be achieved. In this manner, the scaling factor a user can again achieve a link that is entirely compatible with ADSL protocols, and yet is optimized for the particular computing platform initiating the link. Furthermore, the receive and transmit data rates can be controlled entirely by software updates and modifications, rather than by hardware changes, which is an extremely desirable characteristic from the perspective of the user of such device.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a pictorial depiction of the ADSL/DMT bandwidth allocation for upstream and downstream data in a channel based on frequency division multiplexing (FDM) configuration.

FIG. **2** is a block diagram of a general implementation of a communications system employing the present invention, adapted for use in an ADSL environment.

DETAILED DESCRIPTION OF THE INVENTION

According to the T1E1.4 ADSL standards, data bits are grouped and processed every 250 μsec. The number of bits that can be processed over one such time frame is the summation of the bits allocated for each subchannel determined from the previous channel response measurement. For a given number of bits assigned to a certain subchannel, quadrature amplitude modulation (QAM) is used to convert

bits to a complex value, which is then modulated by the subchannel carrier at the corresponding frequency. The general circuits used in prior art ADSL systems are well-known in the art, and will not be discussed at length herein except where such structures or procedures have been modified in accordance with the teachings herein.

The full downstream data throughput of a typical prior art ADSL standard transceiver approaches 6 Mbps, which is more than 200 times the speed of conventional analog modem technology. This requirement was imposed since a large part of the initial motivation to implement ADSL was to achieve high speed multimedia communications and video teleconferencing.

Nevertheless, a large number of potential users cannot or do not need to achieve such wide bandwidth capability. For example, most contemporary (and contemplated) hand-held computing devices are not likely to include extremely powerful onboard digital signal processing capability even though such devices are expected to be interfaced to some degree with xDSL links. Other potential users of ADSL (or similar high speed loops), including many who are intending to use such links primarily for Internet access, only need to achieve downstream transmission speeds that are in the hundreds of kilobits per second range. This data rate is in fact achievable using only a fraction of the available bandwidth of ADSL.

By scaling the data rate in a controlled fashion, the present invention permits a data rate limited ADSL link to be effectuated with significantly less expense and complexity than previously possible. At the same time, because the present invention is flexibly upgraded, the proposed implementation of the present invention affords users an easy path to forward and upward expansion of the overall functionality of their system. The present invention adjusts the data rate of an xDSL link by providing two time scaling factors M and M' in the receive and transmit directions respectively. These two factors are determined by estimating available signal processing power of a communications system to represent the fractional capabilities of the particular transceiver in question compared to a nominal full xDSL data rate implementation. After these factors are determined, they are communicated to an upstream transceiver during a handshaking procedure so that any data link established is data rate constrained to match the downstream transceiver's signal processing capability. As the signal processing capability available to the transceiver is enhanced (either through an upgraded dedicated processor or additional computation horsepower provided by a host processor), the scaling factor M and M' can be reduced, resulting in an increase in the data rate for the link.

GENERAL EMBODIMENT OF PRESENT INVENTION

The basic structure of the present invention is depicted generally in FIG. **2**. In general, the present invention can be embodied in different combinations of hardware and software. The primary difference between these embodiments is the specific implementation of the DMT core, and this is discussed in more detail below.

The structure and operation of ADSL transceivers is well-known in the art, and for that reason the present description primarily details those aspects of such transceivers which are necessary to an understanding of the inventions herein. As seen in FIG. **2**, a channel **100** is made of a regular copper wire "loop", and each such loop may have differing electrical properties, transmission lengths (sizes), varying attenuation characteristics, and a number of impairments or interferences. Splitter **210**, a conventional and well-known circuit, separates a DMT signal occupying more than 200 sub-channels from a lower end 4 kHz POTS analog signal. The latter can be used for simultaneous voice or conventional analog modem transmission. It will be appreciated as well by skilled artisans, however, that the present invention is also completely compatible with so-called "splitterless" ADSL solutions. Hybrid circuit **220** is also well-known in the art, and consists primarily of conventional transformers and isolation circuitry used in a wide variety of high-speed devices interfacing to standard telephone lines. A ring detect logic circuit **290** can also be implemented using accepted techniques, to alert a Control Interface **245** to the existence of a transmission signal originating from an upstream transceiver (not shown).

The full bandwidth signal is bandpass limited to a frequency width B by suitable, well-known techniques as it passes through bandpass Filter and Analog/Digital Converter **280**. The received DMT signal is sampled (using any of a number of well-known techniques) and buffered in Buffer **270**, which, in a preferred embodiment, is a FIFO. This FIFO is large enough to hold a single block of samples for one DMT symbol. Alternatively, it may be desirable in some contexts for Buffer **270** to include a larger FIFO that is capable of holding more than one DMT sample at a time.

Based on a scaling factor M determined during the handshaking process during the time the xDSL link is established with an upstream transceiver, Buffer **270** stores only one DMT symbol from every set of M symbols received. That is, of the M symbols, M−1 symbols are not stored but simply discarded. This scales down the processing load of Receiver Core **260** by a factor of M.

DMT Receiver Core **260** is responsible for extracting the original data stream from the numerous sub-carriers within any specific received DMT symbol block. Based on a scaling factor M negotiated between transceiver **200** and an upstream transceiver, DMT Receiver Core **260** will only process one out of every M received blocks of DMT symbols. The remaining M−1 frames are ignored or dropped as depicted visually in FIG.2. This aspect of the invention results in the fact that the signal processing capability required is reduced correspondingly by a factor M. In a preferred embodiment, M can be practically varied in integral values from 1 to 10, and is preferably an integer between 1 and 6. The additional M−1 frames can be dropped of course since they are merely duplicates of each other transmitted by the upstream transceiver. In this manner, the effective data rate of the xDSL link is scaled down by a factor M. In the limiting case, M=1, and a full xDSL data rate can be achieved. In other words, a reduced received data rate R(Rx)/M is effectuated where R(Rx) is the nominal maximum downstream data rate available in the particular xDSL protocol being used.

Again in a preferred embodiment, Control Interface **245** receives system configuration information from a host through bus **201**. This information may contain such parameters as target throughput rate R, target error rate, etc. By evaluating the signal processing capability of DMT receive core **260**, and taking into consideration a requested target data rate R, Control Interface **245** can determine M prior to data transmission. Again, unlike the prior art, the feedback information concerning M is provided by transceiver **200** based primarily on the limiting factor of signal processing capabilities available at transceiver **200** to implement the DMT Rx and Tx data pumps, and not with regard to the transmitting capacity of the upstream transceiver, or the

bandwidth of channel **100**. This is because, under typical operating conditions, the upstream transceiver and the channel in an xDSL link are expected to have significantly higher data rates.

The DAC **230** and Buffer **240** in the front end transmitting circuit can preferably transmit upstream data using a second frequency bandwidth different from that of the downstream transmission. However, this is not necessary in systems using echo-cancellation. In ADSL applications, the size of this bandwidth is considerably smaller to support a much smaller number of sub-channels. A major modification of this invention to a conventional xDSL transceiver is the fact that Buffer **240** is filled with M' times of the same transmitted DMT symbol. Because of the disparate transmit and receive rates in xDSL systems (such as ADSL), the M and M' values can be different. The scaling factor M' on the transmit side is determined based on the signal processing capability available to process DMT symbols. As such symbols are generated by DMT Tx Core **250**, they are stored in Buffer **240** and then converted to analog wave forms by DAC **230**. In another preferred embodiment, Buffer **240** only needs to store one DMT block and DAC **230** can be controlled by conventional hardware or software logic to repetitively read Buffer **240** M' times. This scaling reduces the load of DMT Tx core **250** by a factor of M', and reduces the transmit data rate to R(Tx)/M', where R(Tx) is the nominal maximum upstream data rate available in the particular xDSL protocol being used.

In a preferred mode of operation, therefore, scaling factors M and M' are first determined for transceiver **200**. Generally speaking, these factors are determined by measuring the time required for the available digital signal processing to process a complete frame, taking into account other typical overhead requirements. This determination procedure can take the form of a self-test or calibration routine that is entirely embedded within a control routine associated with a DSP onboard such transceiver, or, alternatively, in a software modem application, as part of a control routine executed by an off-board processor associated with a user's computing system. It may be desirable, in some contexts to permit a user to configure the specific allocation of transmit and receive data rates through a conventional software program running on such user's personal computer. These routines can be implemented in any number of known ways, and examples are provided in the prior applications noted above. The values for M and M' (which could also include a range of minimum and maximum values for such factors, and/or a relationship between M and M') can be stored onboard transceiver **200** or within an off-board computing system.

When it is desired to establish an xDSL compatible link, standard hand-shaking protocols are utilized such as specified in the T1.413 standard. In addition, however, the upstream transceiver is notified and given information concerning the data rate scaling factors M and M' that transceiver **200** wishes to use for the particular link. Assuming the upstream transceiver contains compatible handshaking processing logic, it can either notify downstream transceiver **200** of the acceptability of such request, or alternatively, in turn request a modification of such factors based on an evaluation of such items as channel characteristics, the target data rates, the processing power available at the upstream transceiver, etc. If the linked transceivers are otherwise able to agree on a set of scaling values M and M', the resulting link is set up to operate in the manner described above.

Some special features of the present invention include the fact that:

(i) unlike hardware architectures implementing a full T1.413 ADSL standard, the present invention loads a DMT block in the receive Buffer **270** every M DMT symbols, where M is agreed to during a handshaking procedure between the upstream and downstream transceivers;

(ii) DMT Rx core **260** is basically implemented the same way as specified by T1.413, but with some important differences, including the fact that it is only necessary to process one of every M DMT symbol blocks within the standard xDSL time period, the speed of FFT implementation can be slower and more cost-effective;

(iii) Control logic **245** permits the system to behave essentially like a conventional analog modem, and is used to support necessary setup tasks such as dialing and handshaking;

(iv) The sampling clock rate, the DMT symbol rate, pilot tones, and upstream and downstream frequency bands remain unchanged from a typical xDSL implementation. The number of samples per symbol, as well as the time duration of a symbol, are also kept the same. These facts make the present invention extremely attractive as a flexible adaptation of xDSL technologies.

(v) The characteristics of a software xDSL transceiver (as discussed in more detail below), including receive and transmit data rates, can be controlled entirely by software updates and modifications to the DMT Tx and Rx routines, rather than by hardware changes.

Other variations which maximize the utility of available signal processing power are apparent. For example, it is conceivable that in some applications it will be desirable to determine a range of values for M and M', and/or to control the relationship between M and M'.

Other variations, which maximize the utility of available signal processing power, are apparent. For example, it is conceivable that in some applications it will be desirable to determine a range of values for M and M' and/or to control the relationship between M and M'. For example, it may be preferable to set M=M' so that the total time spent for each DTM symbol processing is a small fraction of the symbol period. Alternatively, M and M' can be set to maximize either the transmission rate or the receive rate while keeping the total computation time within a small fraction of the overall system load. For example, to maximize the transmission rate, the scaling factor M for the receiver is set to the maximal allowable value and M' for the transmitter is minimized so that the total computation load is within a small fraction of the overall system load. A similar process can be performed when the receive rate needs to maximized. Another possible criterion for setting up the scaling factors is to maintain a certain transmission and receive rate ratio while minimizing the overall load. In this case, the total load

$$\mu = \frac{L_{tx}}{M'} + \frac{L_{rx}}{M}$$

is minimized (L_{tx} and L_{rx} are the computation load for the transmitter and receiver, respectively) while the data rate ratio

$$\frac{R_{tx}/M'}{R_{rx}/M} = C$$

is maintained at a constant C.

The data transmit and receive rates of the transceiver system therefore could be finely controlled and allocated according to the characteristics, needs or desires of any particular user of such system. Moreover, by providing and storing a range of scaling values for M and M', say 3<M<6, and 4<M'<8, a data link can be flexibly and quickly established without the need for further calibrations or processing power determinations.

While DMT Tx Core **250** and DMT Rx Core **260** are shown coupled closely to the front end stages of transceiver **200**, in what may be considered a dedicated hardware implementation, it is apparent that they could also be embodied within a host computing system as part of a "software" modem as explained in more detail below and in the previously filed applications mentioned above. Briefly, however, in a dedicated hardware type implementation DMT sub-channel modulation core is implemented completely in dedicated processing hardware. For this application, DMT Receiver Core **260** typically includes a digital signal processor (DSP) (not shown) and including on-board program ROM (or other suitable memory) for storing executable microcode routines for performing bit, energy and SNR measurements of the carriers in the sub-channels. In such cases system **200** is typically incorporated on a printed circuit board. By mounting or packaging the circuits used in such blocks in an accessible fashion, they can be replaced or supplemented much in the same way present users of personal computers can upgrade their motherboards to include additional microprocessing power or DRAM enhancements. One practical alternative, for example, would be to have an available zero insertion force (ZIF) socket for replacing the DSP or additional available slots to accommodate new DSPs so that a greater number of frames can be processed within a particular time period by DMT Rx Core **260** and DMT Tx Core **250**. Other practical and simple variations of this approach will be apparent to those skilled in the art.

In the above dedicated hardware embodiment, the overall speed (data throughput) can be maximized but with less flexibility for upgrades. This is because upgrades to such a system must take the form of hardware replacements, which can be more costly and difficult for the user to incorporate. On the other hand a number of important functions of a communications system can be completely implemented in software, in an analogous fashion to what is commonly described in the art as a "software" modem. In this case, the overall speed of the system depends on the user's processor power available to such user, and only the AFE and Buffer portions of the transceiver need be implemented in hardware. Such software modem implementations could be used in a personal computer system, a hand-held personal digital assistant, a cellular telephone, and similar portable devices having available signal processing capability.

The primary differences between such embodiments are generally: (1) implementation of DMT modulation; (2) implementation of the control and handshaking functions; and (3) implementation of the control interface. An example of both dedicated hardware and software embodiments of an xDSL transceiver is provided in the above-referenced applications, and either of such embodiments could be used effectively with the present invention. Moreover, a more detailed characterization of preferred embodiments of device drivers and user application programs that could control transceiver **200** are also provided in such applications.

Although the present invention has been described in terms of a preferred ADSL embodiment, it will be apparent to those skilled in the art that many alterations and modifications may be made to such embodiments without departing from the teachings of the present invention. For example, it is apparent that the present invention would be beneficial used in any xDSL or high speed multi-carrier application environment Other types of VLSI and ULSI components beyond those illustrated in the foregoing detailed description can be used suitably with the present invention. Accordingly, it is intended that the all such alterations and modifications be included within the scope and spirit of the invention as defined by the following claims.

What is claimed is:

1. A scalable data rate transceiver comprising:

a channel interface circuit for coupling to and receiving an analog data signal from a data channel; and

a front end receiving circuit for sampling the analog data signal and generating digital signal blocks based on such analog data signal; and

a data buffer coupled to the front end receiving circuit which is adapted to be loaded M consecutive times with a selected one of said digital signal blocks, such that said selected one of said digital signal blocks is used during each of the M loadings, where M has a value>= 1;

a signal processing circuit, which circuit is configurable so that it can process one of the M digital signal blocks from the M loadings;

wherein a data rate R achievable in the data channel is scaled by the value of M resulting in an effective rate R/M achieved by said transceiver.

2. The transceiver of claim **1**, wherein the signal processing circuit is configured to transmit the value of M to an upstream transceiver during a data link initialization procedure so that a data link is configurable using the data rate R/M.

3. The transceiver of claim **2**, wherein the value of M is adjustable to a value Mn (Mn>M) in response to feedback information from the upstream transceiver so that a data rate R/Mn is achieved.

4. The transceiver of claim **1**, wherein data rate R/M is a received data rate used for data received from an upstream transceiver, and a second data rate R'/M' is used for data transmitted from said scalable data rate transceiver to the upstream transceiver, where R' is a maximum available transmission rate, and M' is an integer>=1.

5. The transceiver of claim **4**, wherein the received data rate and transmitted data rate are independently controllable by varying such values of M and M'.

6. The transceiver of claim **5**, wherein a signal processing circuit computation load L_{rx} is needed for processing a received data symbol, and a signal processing circuit computation load L_{tx} is needed for processing a transmitted data symbol; and wherein a data rate ratio (R/M)/(R'/M') is maintained substantially constant while a data load

$$\mu = \frac{L_{tx}}{M'} + \frac{L_{rx}}{M}$$

is minimized.

7. The transceiver of claim **1**, wherein the value of M is configurable as an integer value including from 1 to 10.

8. A high speed communications data receiver for receiving data from an upstream transceiver that is configured to transmit a data stream up to a data rate R, the receiver comprising:

a channel interface circuit for coupling to and receiving said data stream having said rate R; an analog front end circuit for data sampling analog signals, and generating digitals;

a digital signal storage buffer for storing one of every M generated digital signals such that an effective received data rate R/M is achieved, where M is a data rate scaling factor and has an integer value>=1;

a bus interface circuit for transmitting the stored digital signal to a host processing device, and for receiving a transmission control signal from the host processing device to cause said upstream transceiver to transmit at a data rate substantially equal to said data rate R/M during any data stream transmission;

wherein signal processing requirements of said receiver are reduced because processing is only performed on one of every M digital signals.

9. The receiver of claim **8**, wherein the value of M is selected for said receiver based on signal processing capabilities of the host processing device that are available to said receiver.

10. The receiver of claim **9**, wherein a calibration routine executed by the host processing device determines the processing capabilities available to the host processing device, as well as said value for said data rate scaling factor M.

11. The receiver of claim **9**, wherein the value of M is configurable by a user of the host processing device based on system parameter options presented to the user by an applications program running on the host processing device.

12. The receiver of claim **8**, wherein the data receiver is adapted to transmit the value of M to an upstream transceiver during a data link initialization procedure so that a data link can be established using the data rate R/M.

13. The receiver of claim **8**, wherein data rate R/M is a received data rate used for data received from an upstream transceiver, and a second data rate R'/M' is used for data transmitted from said scalable data rate receiver to the upstream transceiver, where R' is a maximum available transmission rate, and where M' is an integer>=1.

14. The receiver of claim **13**, wherein the received data rate and transmitted data rate are independently controlled by varying such values of M and M'.

15. The receiver of claim **14**, wherein a host processing device computation load L_{rx} is needed for processing a received data symbol, and a host processing device computation load L_{tx} is needed for processing a transmitted data symbol; and wherein a data rate ratio (R/M)/(R'/M') is maintained substantially constant while a data load

$$\mu = \frac{L_{tx}}{M'} + \frac{L_{rx}}{M}$$

is minimized.

16. The receiver of claim **8**, wherein M is configurable as an integer value including from 1 to 10.

17. A high speed communications system comprising:

a channel interface circuit for coupling to and receiving an analog data signal from a channel; and

a front end receiving circuit for processing said analog data signal and converting it to a digital signal; and

a digital signal storage buffer for receiving M substantially identical copies of such digital signal, where M is a data rate scaling factor and has an integer value>=1;

a bus interface circuit for transmitting the stored digital signal to a host processing device, and for receiving a transmission control signal from the host processing device to cause a remote transmitter to transmit at a data rate substantially equal to a data rate R/M during any data stream transmission, where R represents a data rate used by said remote transmitter;

wherein the value of M is based on computing capabilities of the host processing device.

18. The system of claim **17**, wherein the value of M is selected for said system based on signal processing capabilities of the host processing device that are available to said system.

19. The system of claim **17**, wherein a calibration routine executed by the host processing device determines the processing capabilities available to the host processor circuit, as well as said value for said data rate scaling factor M.

20. The system of claim **17**, wherein the value of M is configurable by a user of the host processing device based on system parameter options presented to the user by an applications program running on the host processing device.

21. The system of claim **17**, wherein the system is adapted to transmit the value of M to said remote transmitter during a data link initialization procedure so that a data link is configurable using the data rate R/M.

22. The system of claim **17**, wherein data rate R/M is a received data rate used for data received from an upstream transceiver, and a second data rate R'/M' is used for data transmitted from said system to said remote transmitter, where R' is a maximum available transmission rate, and where M' is an integer>=1.

23. The system of claim **17**, wherein the received data rate and transmitted data rate are independently controlled by varying such values of M and M'.

24. The system of claim **22**, wherein a host processing device computation load L_{rx} is needed for processing a received data symbol and a host processing device computation load L_{tx} is needed for processing a transmitted data symbol; and wherein a data rate ratio (R/M)/(R'/M') is maintained substantially constant while a data load

$$\mu = \frac{L_{tx}}{M'} + \frac{L_{rx}}{M}$$

is minimized.

25. The system of claim **17**, wherein M is configurable as an integer value including from 1 to 10.

26. A data rate scalable xDSL software transceiver comprising:

a channel interface circuit for coupling to and receiving an analog data signal from a digital subscriber loop data channel; and

a front end receiving circuit for sampling the analog data signal and generating a digital DMT symbol based on such analog data signal; and

a data buffer coupled to the front end receiving circuit which from every set of M consecutive DMT symbols generated by the front end circuit generates a single DMT symbol; and

a bus interface circuit for transmitting the stored DMT symbol to a host processing device, and for receiving a transmission control signal from the host processing device to cause a remote transceiver to transmit at a data rate substantially equal to a data rate R/M during any data stream transmission, where R is a maximum data rate for said remote transceiver;

wherein a value for M is adjustable by said transceiver based on characteristics of the host processing device,

and said data rate of said transceiver is controllable based on the value for M.

27. The transceiver of claim 26, wherein the value of M is selected based on signal processing capabilities of the host processing device.

28. The transceiver of claim 26, wherein the value of M is configurable by a calibration routine executed by the host processing device to determine the processing capabilities available to the host processing device.

29. The transceiver of claim 26, wherein the value of M is configurable by a user of the host processing device based on system parameter options presented to the user by an applications program running on the host processing device.

30. The transceiver of claim 26 wherein data rate R/M is a received data rate used for data received from said remote transceiver, and a second data rate R'/M' is used for data transmitted from said scalable data rate transceiver to the remote transceiver, where R' is a maximum available transmission rate and where M' is an integer>=1.

31. The transceiver of claim 30, wherein the received data rate and transmitted data rate are independently controlled by varying such values of M and M'.

32. The transceiver of claim 31, wherein a signal processing circuit computation load L_{rx} is needed for processing a received data symbol, and a signal processing circuit computation load L_{tx} is needed for processing a transmitted data symbol; and wherein a data rate ratio (R/M)/(R'/M') is maintained substantially constant while a data load

$$\mu = \frac{L_{rx}}{M'} + \frac{L_{rx}}{M}$$

is minimized.

33. The transceiver of claim 26, wherein M is configurable as an integer value including from 1 to 10.

34. A data rate scalable xDSL transceiver comprising:

a channel interface circuit for coupling to and receiving an analog data signal from a digital subscriber loop data channel; and

a front end receiving circuit for sampling the analog data signal and generating a digital DMT symbol based on such analog data signal; and

a data buffer coupled to the front end receiving circuit which from every set of M consecutive DMT symbols generated by the front end circuit generates a single DMT symbol; and

a signal processing circuit for processing the single DMT symbol;

wherein a value for M is configurable based on characteristics of the signal processing circuit, and a data rate R/M of the data rate scalable transceiver is controllable based on the value for M, where R is a data rate used by a remote transceiver and

further wherein the data rate scalable xDSL transceiver is configured to transmit the value of M to said remote transceiver during a data link initialization procedure.

35. The transceiver of claim 34 wherein M is configurable as an integer value including from 1 to 10.

36. The transceiver of claim 35, wherein the value of M is selected for said transceiver based on signal processing capabilities of the signal processing circuit.

37. A data rate scalable xDSL transceiver comprising:

a channel interface circuit for coupling to and receiving an analog data signal from a digital subscriber loop data channel; and

a front end receiving circuit for sampling the analog data signal and generating a digital DMT symbol based on such analog data signal; and

a data buffer coupled to the front end receiving circuit which from every set of M consecutive DMT symbols generated by the front end circuit generates a single DMT symbol; and

a signal processing circuit for processing the single DMT symbol;

wherein a value for M is configurable based on characteristics of the signal processing circuit, and a data rate of the transceiver is controllable based on the value for M; and

further wherein a received data rate R/M is used for data received from a remote transceiver, where R is a maximum transmit data rate for said remote transceiver, and a second data rate R'/M' is used for data transmitted from the data rate scalable xDSL transceiver to said remote transceiver, where R' is a maximum available transmission rate for the data rate scalable xDSL transceiver, and where M' is an integer>=1.

38. A data rate scalable xDSL transceiver comprising:

a channel interface circuit for coupling to and receiving an analog data signal from a digital subscriber loop data channel; and

a front end receiving circuit for sampling the analog data signal and generating a digital DMT symbol based on such analog data signal; and

a data buffer coupled to the front end receiving circuit which from every set of M consecutive DMT symbols generated by the front end circuit generates a single DMT symbol; and

a signal processing circuit for processing the single DMT symbol;

wherein a value for M is configurable based on characteristics of the signal processing circuit, and a data rate of the transceiver is controllable based on the value for M; and

further wherein a received data rate R/M is used for data received from a remote transceiver, where R is a maximum transmit data rate for said remote transceiver, and a second data rate R'/M' is used for data transmitted from the data rate scalable xDSL transceiver to said remote transceiver, where R' is a maximum available transmission rate for the data rate scalable xDSL transceiver and where M' is an integer>=1:

whereby the received data rate and transmitted data rate are independently controlled by varying such values of M and M'.

39. A data rate scalable xDSL transceiver comprising:

a channel interface circuit for coupling to and receiving an analog data signal from a digital subscriber loop data channel; and

a front end receiving circuit for sampling the analog data signal and generating a digital DMT symbol based on such analog data signal; and

a data buffer coupled to the front end receiving circuit which from every set of M consecutive DMT symbols generated by the front end circuit generates a single DMT symbol; and

a signal processing circuit for processing the single DMT symbol;

wherein a value for M is configurable based on characteristics of the signal processing circuit, and a data rate of the transceiver is controllable based on the value for M; and

further wherein a received data rate R/M is used for data received from a remote transceiver, where R is a

maximum transmit data rate for said remote transceiver, and a second data rate R'/M' is used for data transmitted from the data rate scalable xDSL transceiver to said remote transceiver, where R' is a maximum available transmission rate for the data rate scalable xDSL transceiver, and where M' is an integer>=1, such that the received data rate and transmitted data rates are independently controlled by varying such values of M and M; and

further wherein when a computation load L_{rx} is needed for processing a received symbol, and a computation load L_{tx} is needed for processing a transmitted symbol, a data rate ratio (R/M)/(R'/M') is maintained substantially constant while a data load

$$\mu = \frac{L_{tx}}{M'} + \frac{L_{rx}}{M}$$

is minimized.

40. A data rate scalable transceiver configured to be used in a digital subscriber loop supporting a downstream data transmission rate R and an upstream data transmission rate R', said transceiver comprising:

an interface circuit for coupling to and receiving an analog data signal from said digital subscriber loop; and

a front end receiving circuit for sampling the analog data signal and generating a received digital DMT symbol based on such analog data signal; and

a receive data buffer coupled to the front end receiving circuit which from every set of M consecutive DMT symbols generated by the front end circuit generates a single DMT symbol, where M has an integer value>=1; and

a signal processing circuit for processing the single received DMT symbol, and for generating a sequence of M' identical DMT symbols containing data to be transmitted by said transceiver, where M' has an integer value>=1; and

a transmit data buffer for storing the M' identical DMT symbols from the signal processing circuit; and

a front end transmitting circuit for generating an analog transmission data signal based on the M' DMT symbols; and

wherein said downstream data transmission rate R is scaled to a rate R/M, and said upstream data transmission rate R' is scaled to a rate R'/M'.

41. The transceiver of claim **40**, wherein the values of M and M' are selected for said transceiver based on signal processing capabilities of the signal processing circuit.

42. The transceiver of claim **40**, wherein the transceiver is configured to transmit the values of M and M' to an upstream transceiver during a data link initialization procedure so that a data link is configurable using the downstream data transmission rate R/M and upstream data transmission rate R'/M'.

43. The transceiver of claim **40**, wherein a computation load L_{rx} is needed for processing a received data symbol and a computation load L_{tx} is needed for processing a transmitted data symbol; and wherein a data rate ratio (R/M)/(R'/M') is maintained substantially constant while a data load

$$\mu = \frac{L_{tx}}{M'} + \frac{L_{rx}}{M}$$

is minimized.

44. The transceiver of claim **40**, wherein M and M' have variable integer values including from 1 to 10.

45. A method of implementing a scalable data rate transceiver comprising the steps of:

receiving an analog data signal from a data channel; and

sampling the analog data signal and generating a digital signal based on such analog data signal; and

receiving M substantially identical copies of such digital signal, where M is configured to have a value>=1;

processing one of the M copies of the digital signals;

wherein a data rate R achievable in the data channel is scalable by the value of M resulting in an effective rate R/M achieved by said transceiver.

46. The method of claim **45**, wherein the value of M is based on computing capabilities of a signal processing circuit used for processing the digital signals.

47. The method of claim **45**, further including a step transmitting the value of M to an upstream transceiver during a data link initialization procedure so that a data link is established using the data rate R/M.

48. The method of claim **45**, further including a step of adjusting M to have a value Mn (Mn>M) in response to feedback information from an upstream transceiver so that a data rate R/Mn is achieved.

49. The method of claim **45**, wherein data rate R/M is a received data rate used for data received from an upstream transceiver, and a second data rate R/M' is used for data transmitted from said data rate transceiver to the upstream transceiver, where R' is a maximum available transmission rate, and where M' is an integer>=1.

50. The method of claim **49**, wherein the received data rate and transmitted data rate are independently controlled by varying such values of M and M'.

51. The method of claim **50**, wherein a computation load L_{rx} is needed for processing a received data symbol, and a computation load L_{tx} is needed for processing a transmitted data symbol; and wherein a data rate ratio (R/M)/(R'/M') is maintained substantially constant while a data load

$$\mu = \frac{L_{tx}}{M'} + \frac{L_{rx}}{M}$$

is minimized.

52. The method of claim **45**, wherein M is configurable as an integer value including from 1 to 10.

53. The method of claim **45**, further including a step wherein an ADSL compatible data link is set up by said transceiver in said channel.

54. A method for communicating data to a host processing device from an upstream transceiver transmitting an analog data transmission signal using a nominal data rate R in a channel coupled to the host processing device, said method comprising the steps of:

receiving said analog data transmission signal from the channel; and

processing the analog data transmission signal and generating a corresponding digital signal; and

storing one of every M generated digital signals generated during step (b) such that an effective received data rate R/M is achieved with the upstream transceiver, where M is a data rate scaling factor and has an integer value>=1;

processing said one of every M digital signals; and

generating feedback information indicating to the upstream transceiver that a data rate of R/M should be used in said channel even when said channel can support said data rate R.

55. The method of claim **54**, wherein the value of M is based on computing capabilities of a signal processing circuit used for processing said one of every M digital signals.

56. The method of claim **54**, wherein data rate R/M is a received data rate used for data received from the upstream transceiver, and a second data rate R/M' is used for data transmitted to the upstream transceiver, where R' is a maximum available transmission rate, and where M' is an integer>=1.

57. The method of claim **56**, wherein the received data rate and transmitted data rate are independently controlled by varying such values of M and M'.

58. The method of claim **54**, wherein M and M' are configurable as integer values including from 1 to 10.

59. The method of claim **54**, further including a step wherein an ADSL compatible data link is set up by said transceiver in said channel.

60. A method of operating a high speed communications system that is coupled through a channel to a host processing device and an upstream transceiver supporting an analog data transmission signal having a data rate R, said method comprising:

(a) configuring said system to achieve a receive data rate R/M, where M is a data rate scaling factor and has an integer value>=1; and

(b) receiving an analog initialization signal at said rate R from the upstream transceiver through the channel; and

(c) generating feedback information indicating to the upstream transceiver that a data rate of R/M should be used for data transmission; and

(d) receiving an analog data transmission signal at an effective data rate R/M from the upstream transceiver; and

(e) generating a digital signal based on sampling the analog data transmission signal; and

(f) transmitting the digital signal to said host processing device so that it is processed to extract selected data from the data carrying signals.

61. The method of **60** further including a step: determining an optimal value for M based on processing capabilities of said host processing device.

62. The method of claim **60**, further including a step wherein protocol information pertaining to standards applicable to Asymmetric Digital Subscriber Loops is transmitted by the upstream data transceiver so as to set up an ADSL compatible data link.

63. The method of claim **61**, wherein data rate R/M is a received data rate used for data received from the upstream transceiver, and a second data rate R/M' is used for data transmitted to the upstream transceiver, where R' is a maximum available transmission rate, and where M' is an integer>=1.

64. The method of claim **63**, wherein the received data rate and transmitted data rates are independently controlled by varying such values of M and M'.

65. The method of claim **64**, wherein M and M' are configurable as integer values including from 1 to 10.

* * * * *

Evidence Appendix 3

McGhee

US006658049B1

(12) **United States Patent**
McGhee et al.

(10) **Patent No.: US 6,658,049 B1**
(45) **Date of Patent: Dec. 2, 2003**

(54) **XDSL REPEATER SYSTEM AND METHOD**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/228,688**

(22) Filed: **Jan. 12, 1999**

(51) **Int. Cl.**[7] **H04B 17/02**; H04B 3/36; H04B 7/17; H04C 25/20; H04C 25/52

(52) **U.S. Cl.** **375/211**; 375/222; 370/492

(58) **Field of Search** 375/259, 260, 375/285, 211, 219, 220, 254, 296, 346, 348, 350, 227, 222; 379/417; 370/201, 203, 210, 352, 484, 487, 492, 494

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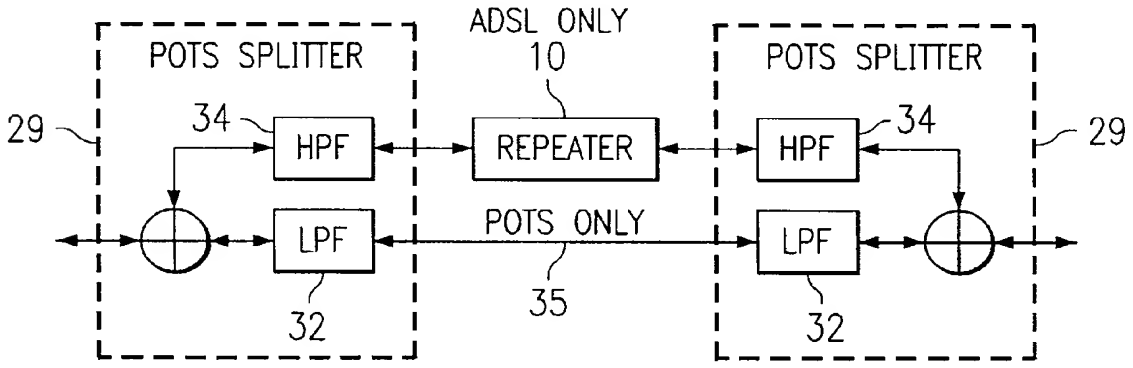
Primary Examiner—Chi Pham
Assistant Examiner—Demetria Williams
(74) *Attorney, Agent, or Firm*—Baker Botts L.L.P.

(57) **ABSTRACT**

A system for repeating an xDSL signal (**14**) is disclosed. The system comprises a receiver (**16**) operable to receive the xDSL signal (**14**), a first analog front end (**18**) coupled to the receiver (**16**) and operable to convert the xDSL signal to a digital signal, and a series of digital signal processors (**20**, **22**) coupled to the first analog front end (**18**) and operable to remove noise elements from the digital signal. Also provided is a second analog front end (**24**) coupled to the second digital signal processor (**22**) and operable to convert the digital signal back to the analog domain. A driver circuit (**26**) is operable to increase the signal strength of the analog signal and retransmits it over a new length of wiring.

12 Claims, 1 Drawing Sheet



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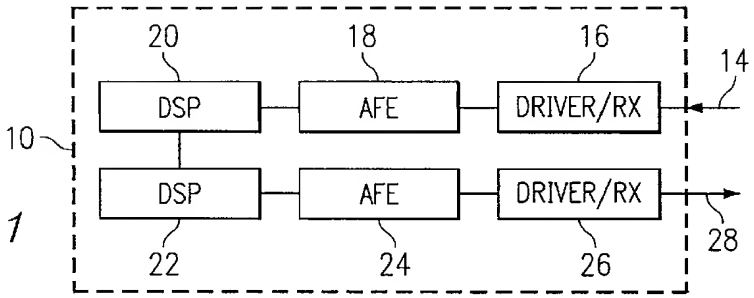

FIG. 1

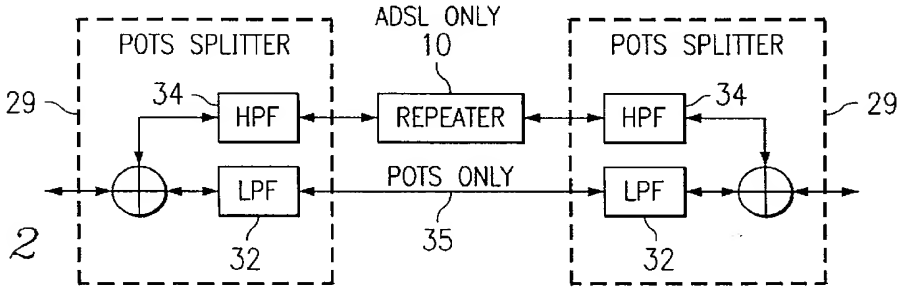

FIG. 2

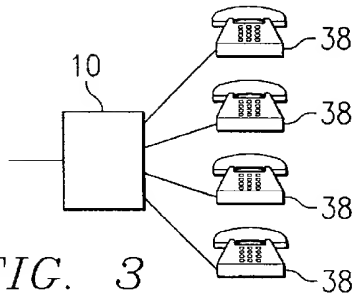

FIG. 3

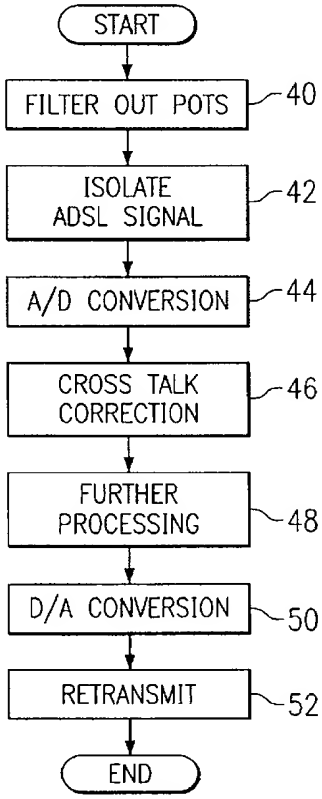

FIG. 4

XDSL REPEATER SYSTEM AND METHOD

TECHNICAL FIELD OF THE INVENTION

This invention relates to the field of telecommunication and more specifically to an xDSL repeater system and method.

BACKGROUND OF THE INVENTION

As demand for broadband services, such as high speed Internet access and on-demand video to the home increases, the need for technologies that can transmit large bandwidths of information also increases.

One technology being introduced to fill this need is digital subscriber lines (xDSL). The advantage of xDSL over other broadband technologies such as fiber optics to the home or cable modems is that it uses the existing twisted pair copper lines that already provide telephone services to homes.

The term xDSL is a catchall term covering a number of similar technologies. These include High bit rate Digital Subscriber Line (HDSL) and Asymmetric Digital Subscriber Line (ADSL).

HDSL is designed to deliver T1 (1.544 Mbps) and E1 (2.048 Mbps) services over conventional copper lines by using transceivers on each end of two or three twisted pairs. Single pair HDSL is limited to 384 Kbps or 768 Kbps symmetrical speeds.

ADSL uses conventional twisted pair copper lines to provide a large downstream path and a smaller upstream path. This allows for services such as on demand video and high speed Internet access where the user needs to receive greater bandwidth than the user needs to send. In one embodiment, ADSL is capable of providing downstream rates in excess of 6 Mbps and simultaneous duplex transmissions of 640 Kbps. Several competing ADSL standards exist. These include Discrete Multitone (DMT) and Carrierless Amplitude and Phase modulation (CAP). In one embodiment, DMT divides the 1 MHZ phone line spectrum into 256 4 KHz channels. Transmission bit density can be varied to overcome noise and interference.

CAP uses a single carrier and utilizes amplitude modulation similar to that used for modems to achieve ADSL transmission.

Both DMT and CAP operate by placing an ADSL modem on either end of a twisted-pair telephone line (one at a central office and the other at the customer's home or office). Three channels are created: a POTS (plain old telephone service) channel, a medium speed duplex channel and a high speed downstream channel. In a typical embodiment, POTS takes up the first 4 KHz of the phone line spectrum. The medium speed duplex channel and the high speed downstream channel occupy higher frequencies in the spectrum. Since the POTS channel is located in the first 4 KHz of the spectrum it can be split off from the data channels by filtering, thus providing an uninterrupted POTS connection.

One drawback of xDSL systems is that transmission signals attenuate as line length increases. For example, in order to maintain a downstream rate of around 6 Mbps the maximum loop length of copper is 12,000 Feet. This drawback limits the number of homes that can access xDSL service.

SUMMARY OF THE INVENTION

Accordingly, a need has arisen for an xDSL Repeater System and Method. The present invention includes a system and method that provides a xDSL repeater that addresses the shortcoming of prior systems and methods.

According to one embodiment of the invention, a system for repeating an xDSL signal is provided. The system is comprised of two receiver/transmitters. The receivers consists of an analog front end which amplifies and converts the analog signal to the digital domain. The digital data is passed to a digital signal processor which is responsible for time and frequency domain equalization, echo cancellation, and decoding the signal. The transmitters take the decoded data and encode the data, transfer it to the analog front end where it is converted to an analog signal, amplified, and sent down the remainder of the cable to the far end transceiver. Also, a replica of the transmitted signal is transferred to the receiver DSP to remove crosstalk that is induced on the line when the powerful transmitted signal leaves the repeater adjacent to the weaker received signal.

The present invention provides various technical advantages. For example, a repeater is provided that allows for xDSL to reach further distances. Other technical advantages may be readily apparent to one skilled in the art from the following figures, descriptions and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and advantages thereof, reference is now made to the following descriptions taken in conjunction with the following drawings, in which like numbers represent like parts, in which:

FIG. **1** illustrates an xDSL repeater in accordance with the teachings of the present invention;

FIG. **2** illustrates a high pass filter with a repeater in accordance with the teaching of the present invention;

FIG. **3** illustrates an alternative embodiment of the present invention; and,

FIG. **4** is a flowchart illustrating the operation of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Embodiments of the present invention and its advantages are best understood by referring to FIGS. **1** through **4** of the drawings, like numerals being used for like and corresponding parts of the various drawings.

FIG. **1** illustrates a xDSL repeater in accordance with the teaching of the present invention. xDSL repeater **10** comprises a first driver/receiver **16** coupled to a first analog front end **18** coupled to a first digital signal processor (DSP) **20** which is coupled to second DSP **22** which is in turn coupled to a second analog front end **24** which is coupled to a second driver/receiver **26**. FIG. **1** is a schematic drawing showing operational blocks for each, the various functional blocks could actually be implemented as one or more components in an actual embodiment.

In operation, a xDSL signal **14** is received by driver/receiver **16**. Driver/receiver **16** then passes the signal to analog front end **18** which converts the analog signal to a digital signal in order for it to be processed by first DSP **20**. First DSP **20** receives the digital signal from analog front end **18**.

First DSP **20** and second DSP **22** are operable, either singularly or together, to eliminate crosstalk and other noise which can occur in a repeater system. Crosstalk occurs when there is a signal delay in a repeater which is a replica of the regenerated signal that overlays the transmitted signal.

Typically, the longer the loop length, the worse crosstalk can be. Crosstalk also can occur when a bundle of twisted pair wires are provided together. In this case, crosstalk occurs between the different wires in a bundle. First DSP **20** can eliminate crosstalk by monitoring what signal exits second DSP **22** and then finding a preset delay to produce a replica of the transmitted signal (crosstalk) to be subtracted from the received signal. As an alternate, the first DSP **20** can take the received signal, generate its own version of the crosstalk replica and subtract the delayed version from its own input.

Aside from handling crosstalk, DSP **20** and **22** can also perform other signal processing chores such as time or frequency domain transformations, block error corrections using algorithms such as the Reed-Solomon algorithm, or bit error corrections using a Viterbi algorithm or other bit correcting algorithms. These can be done for noise reduction purposes.

After DSPs **20** and **22** have eliminated crosstalk and performed other signal processing chores, the signal is sent to second analog front end **24**. Analog front end **24** converts the digital signal back to an analog signal which is then sent to driver **26**. Driver **26** then transmits the regenerated signal **28** over the next loop of twisted pair wires.

In some cases of extreme crosstalk, analog front end **18** may need to be used to reduce crosstalk in the analog domain by subtracting the analog replica of the outgoing signal.

Additionally, since xDSL lines are capable of carrying a POTS signal, it is important to split off the POTS signal before sending the signal into repeater **10**. FIG. **2** illustrates an exemplary system to filter out POTS signals. POTS Splitter **29** comprises a low pass filter **32** which will allow only frequencies below a certain level to pass. Low pass filter is chosen to allow only the POTS signal to travel along line **35**. POTS splitters **29** are set up on either side of repeater **10** and line **35** since communication can travel in either direction. POTS splitter **29** optionally includes a high pass filter **34** placed before the repeater to ensure only frequencies above the POTS frequency is sent to repeater **10**.

FIG. **3** illustrates another embodiment of the present invention. In FIG. **3** the incoming digital signal **14** is sent to repeater **10**. In this case, repeater **10** is operable to repeat the signal at lower bandwidth rates and send them along different paths to individual homes **38**. This acts like a multiplexer. Like a repeater, it also provides a longer line length, albeit it at a lower transmit and receive rate than a single xDSL loop would have. For example, a six megabit per second link could be divided among several households at a lower rate such as a 750 KHz downstream rate for each home. This approach can also be used in apartment complexes where one xDSL link could be used to provide many subscribers in different apartments with slower rate xDSL lines.

FIG. **4** is a flow chart illustrating the operation of the present invention. As execution of the flow chart begins in step **40**, the POTS line is filtered out. As discussed before, this can be done by means of a high pass filter or other filtering techniques to remove lower frequency POTS line from the upstream and downstream data signals of xDSL. In step **42**, the xDSL signal is isolated. Then, in step **44**, the analog front end completes an analog digital conversion converting the analog data signals into the digital domain. Crosstalk is canceled by DSPs **20** and **22** in step **46**. This can be done as discussed before in several different ways.

The signal is then further processed in step **48**. This further processing can include error correction via a blocking coding process such as a Reed-Solomon process or a bit incrementing process such as that done in Viterbi analysis. Also, time or frequency based transforms may be done for signal processing purposes. Then, in step **50**, the digital signal is converted back to the analog domain and in analog front end. Finally, in step **52**, the signal is then boosted using driver **26** and the now analog signal is repeated and sent over a new loop of twisted pair copper wiring until it reaches either a customer presence equipment or another repeater.

Although the present invention has been describe in detail, it should be understood that various changes, substitutions and alterations can be made thereto without departing from the spirit and scope of the invention as defined by the appended claims.

What is claimed is:

1. A method for repeating an xDSL signal comprising the steps of:

isolating the xDSL signal;

converting the xDSL signal into a digital signal;

removing noise elements;

converting the signal back to an analog signal;

retransmitting the signal; and

wherein the step of removing noise elements comprises removing crosstalk by formulating an appropriately delayed signal image.

2. A method for repeating an xDSL signal comprising the steps of:

isolating the xDSL signal;

converting the xDSL signal into a digital signal;

removing noise elements;

converting the signal back to an analog signal;

retransmitting the signal; and

wherein the step of removing noise elements comprises performing bit error corrections.

3. A system for repeating an xDSL signal comprising:

a receiver operable to receive the xDSL signal;

a first analog front end coupled to the receiver and operable to convert the xDSL signal to a digital signal;

a series of digital signal processors coupled to the first analog front end and operable to remove noise elements from the digital signal;

a second analog front end coupled to each digital signal processor and operable to convert the digital signal back to an analog xDSL signal; and

a driver circuit coupled to each analog front end and operable to increase the signal strength of the analog xDSL signal and retransmit it over a new length of wiring.

4. The system of claim **3**, wherein a POTS signal is removed before noise elements are removed.

5. The system of claim **3**, wherein the digital signal processors are operable to remove noise elements by removing crosstalk by formulating an appropriately delayed replica.

6. The system of claim **3**, wherein the digital signal processors are operable to perform block error corrections.

7. The system of claim **3**, wherein the digital signal processors are operable to perform bit error corrections.

8. The system of claim **3**, wherein the first and second analog front ends are operable to remove crosstalk.

9. The system of claim **3**, wherein the xDSL signal is an ADSL signal.

10. A system for repeating an xDSL signal comprising:

a receiver operable to receive the xDSL signal;

a first analog front end coupled to the receiver and operable to convert the xDSL signal to a digital signal;

a series of digital signal processors coupled to the first analog front end and operable to remove noise elements from the digital signal;

a second analog front end coupled to each digital signal processor and operable to convert the digital signal back to the analog domain;

a driver circuit coupled to each analog front end and operable to increase the signal strength of the analog signal and retransmit it over a new length of wiring; and

wherein the digital signal processors are operable to remove noise elements by removing crosstalk by formulating an appropriately delayed replica.

11. A system for repeating an xDSL signal comprising:

a receiver operable to receive the xDSL signal;

a first analog front end coupled to the receiver and operable to convert the xDSL signal to a digital signal;

a series of digital signal processors coupled to the first analog front end and operable to remove noise elements from the digital signal;

a second analog front end coupled to each digital signal processor and operable to convert the digital signal back to the analog domain;

a driver circuit coupled to each analog front end and operable to increase the signal strength of the analog signal and retransmit it over a new length of wiring; and

wherein the digital signal processors are operable to perform bit error corrections.

12. A system for repeating an xDSL signal comprising:

a receiver operable to receive the xDSL signal;

a first analog front end coupled to the receiver and operable to convert the xDSL signal to a digital signal;

a series of digital signal processors coupled to the first analog front end and operable to remove noise elements from the digital signal;

a second analog front end coupled to each digital signal processor and operable to convert the digital signal back to the analog domain;

a driver circuit coupled to each analog front end and operable to increase the signal strength of the analog signal and retransmit it over a new length of wiring; and

wherein the first and second analog front ends are operable to remove crosstalk.

* * * * *

Evidence Appendix 4

Fisher

United States Patent [19]

Fisher

[11] **Patent Number: 4,878,232**

[45] **Date of Patent: Oct. 31, 1989**

[54] **DATA TRANSMISSION SYSTEM**

[75] Inventor: **David A. Fisher**, Saffron Walden, Great Britain

[73] Assignee: **STC PLC**, London, England

[21] Appl. No.: **919,036**

[22] Filed: **Oct. 15, 1986**

[30] **Foreign Application Priority Data**

Nov. 20, 1985 [GB] United Kingdom 8526610

[51] **Int. Cl.**[4] **H04L 7/04**; H04L 5/14

[52] **U.S. Cl.** **375/111**; 370/32.1; 340/825.2

[58] **Field of Search** 375/60, 99, 103, 111, 375/116; 340/825.05, 825.14, 825.2; 370/32, 32.1

[56] **References Cited**

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4,766,589 8/1988 Fisher 370/32

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2082025 2/1982 United Kingdom .
2161676 1/1986 United Kingdom .

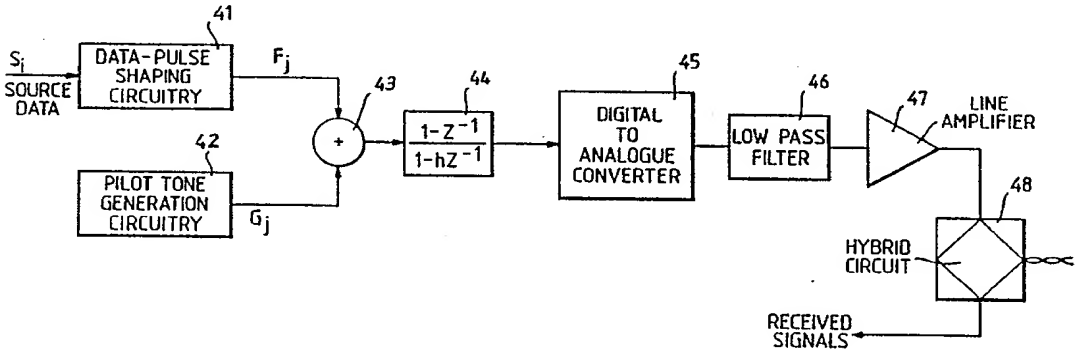
Primary Examiner—Derek S. Jennings

Attorney, Agent, or Firm—Lee & Smith

[57] **ABSTRACT**

In a data transmission system data is sent, after suitable conversion, as a ternary analogue type signal. Using two-wire twisted pairs and hybrids, echo cancellation and feedback equalization are needed. Synchronization between the two ends, e.g. of a 144 Kb/sec. subscriber's loop, is maintained by a low amplitude pilot tone sent with the data, which is detected at the same time as the data is detected. Detection and elimination of this pilot tone use coefficient generation circuitry similar to those used in the equalizer and echo canceller. To reduce the effect of time phase steps on the system performance, in addition to the transmission of a specific zero valued frame synchronization word which immediately precedes the phase step, the incoming synchronization word is also aligned to this time so that the value of a symbol as received can be predicted, as for a synchronization word, the predicted value is given preference if there is a difference between that symbol's value as received and its predicted value. In addition, the location of the high-pass filters used in the system are specified, alternative methods of bit timing control are specified and advantageous realizations of the canceller and equalizer using tap interpolation are disclosed.

16 Claims, 10 Drawing Sheets



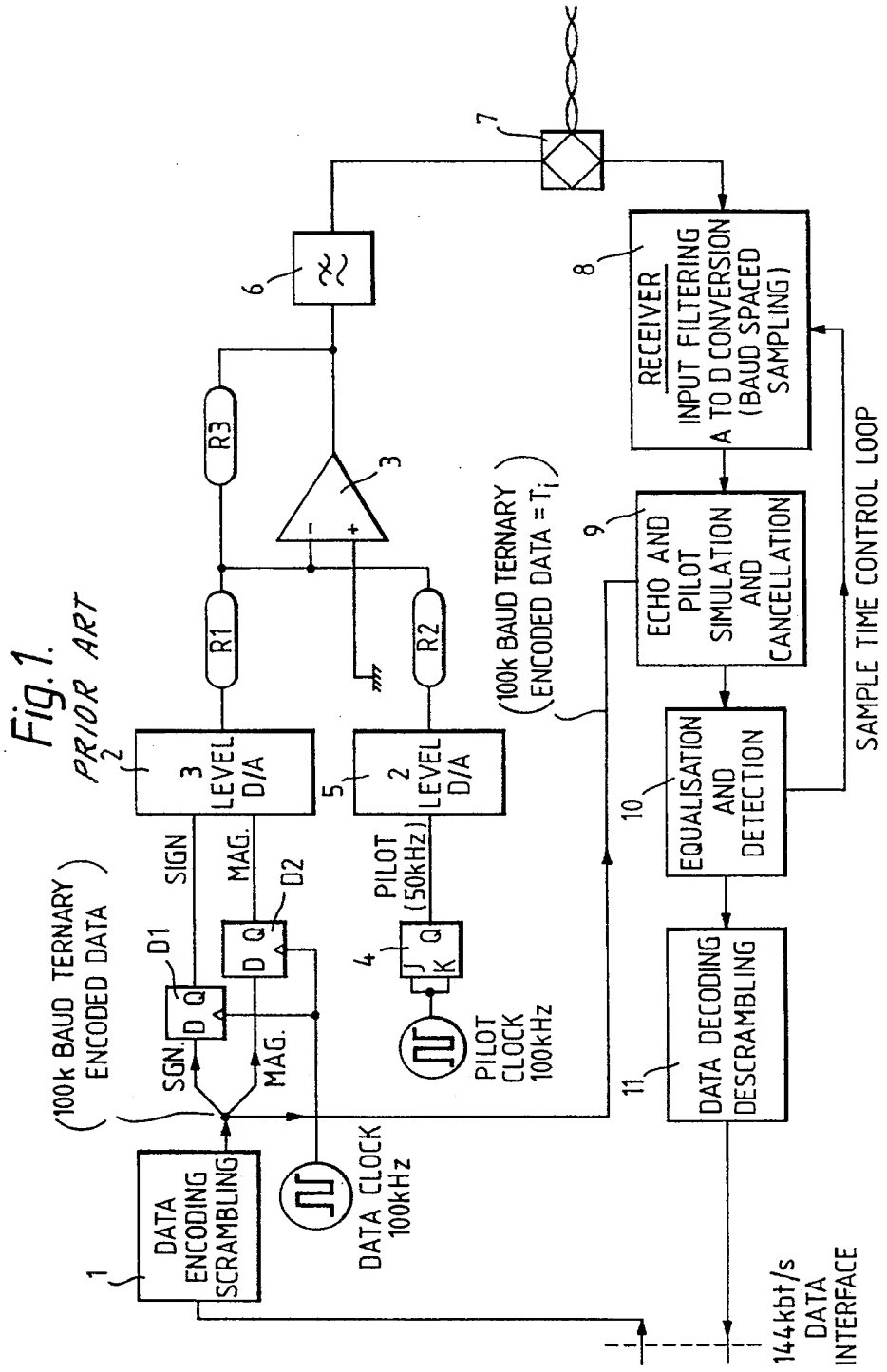


Fig. 1.
PRIOR ART

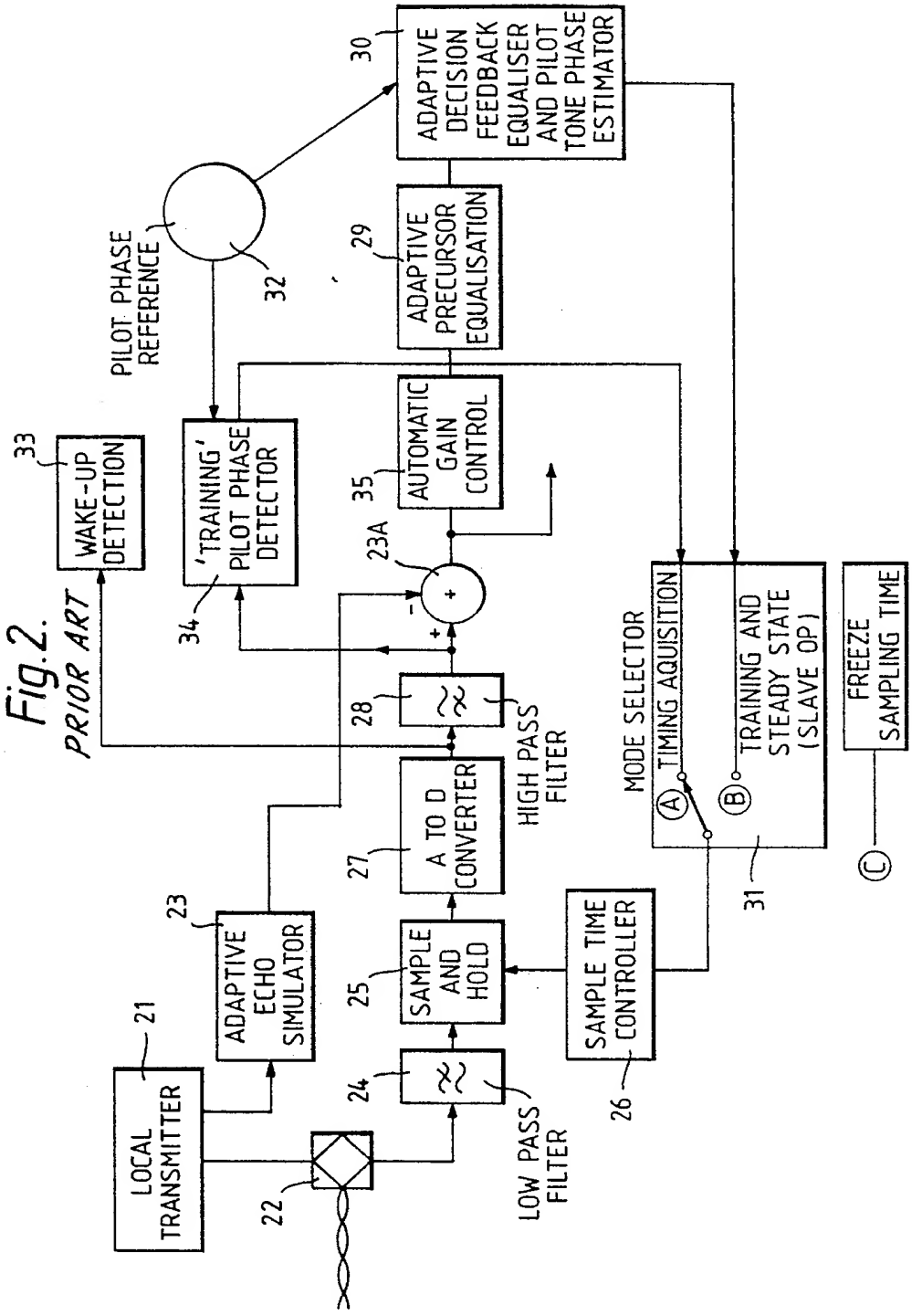


Fig. 2.
PRIOR ART

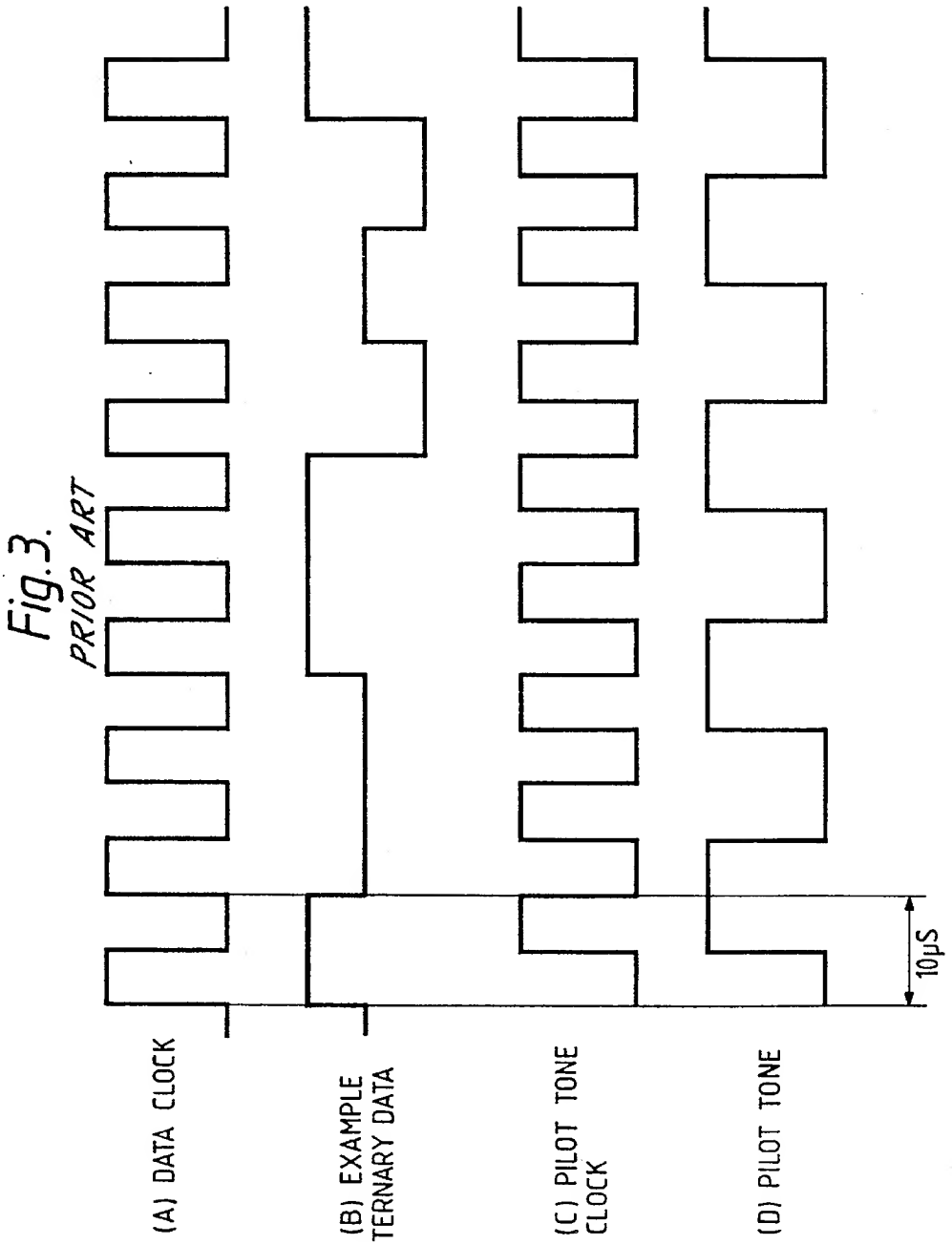


Fig. 3.
PRIOR ART

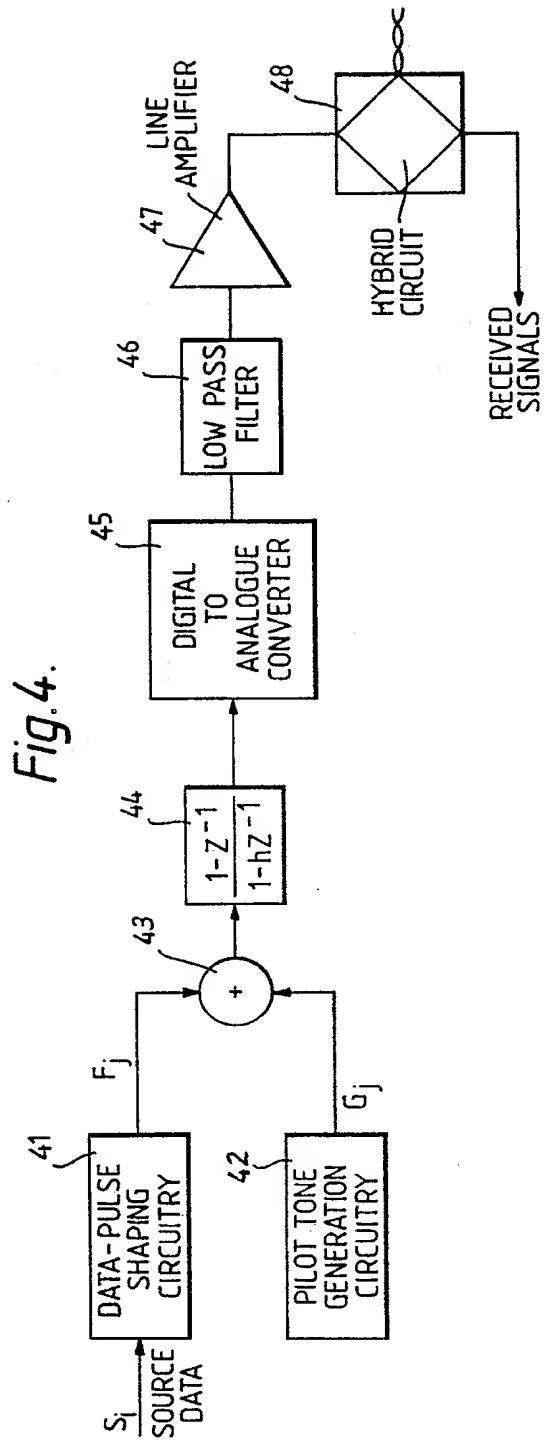

SOURCE DATA
S_i
DATA-PULSE SHAPING CIRCUITRY
41
F_j
PILOT TONE GENERATION CIRCUITRY
42
G_j
43
$\frac{1-Z^{-1}}{1-hZ^{-1}}$
44
DIGITAL TO ANALOGUE CONVERTER
45
LOW PASS FILTER
46
LINE AMPLIFIER
47
HYBRID CIRCUIT
48
RECEIVED SIGNALS

Fig.4.

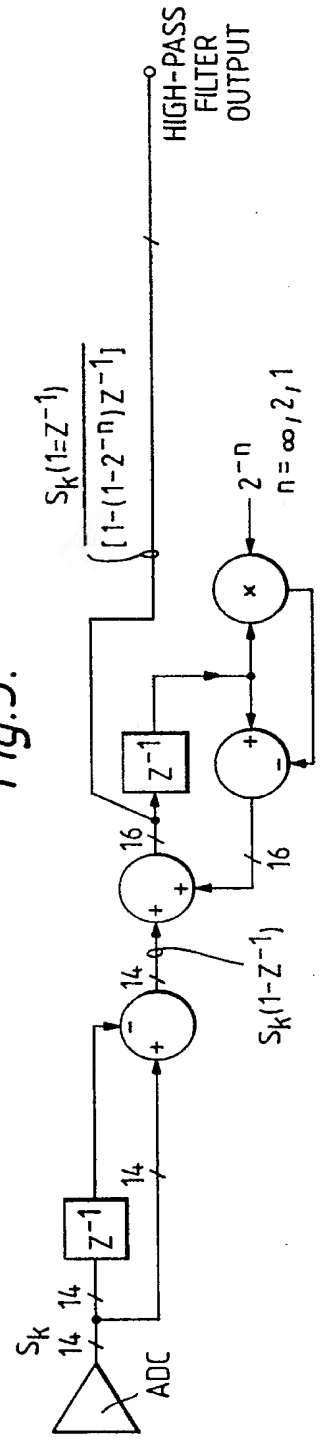
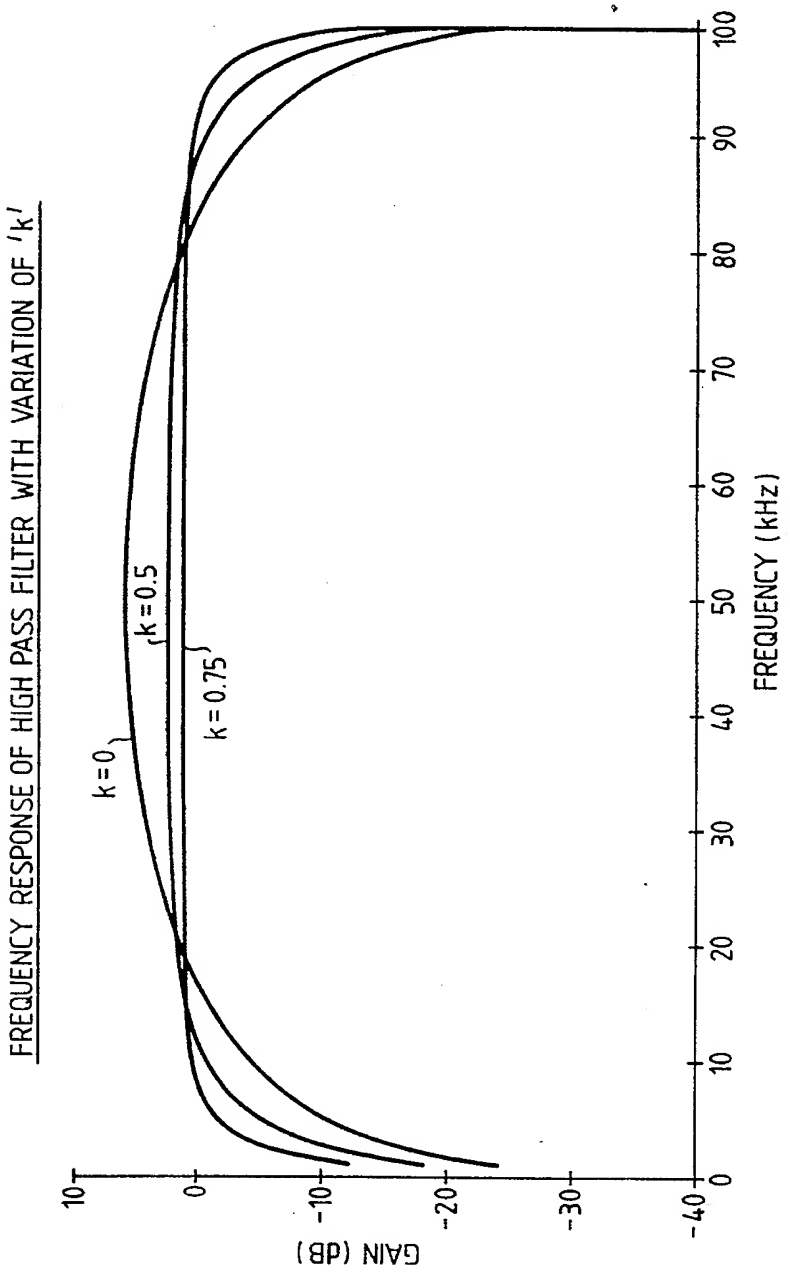

ADC
S_k
14
Z^{-1}
14
14
$S_k(1-Z^{-1})$
16
Z^{-1}
$\frac{S_k(1=Z^{-1})}{[1-(1-2^{-n})Z^{-1}]}$
2^{-n}
$n=\infty, 2, 1$
HIGH-PASS FILTER OUTPUT

Fig.5.

Fig.6.


FREQUENCY RESPONSE OF HIGH PASS FILTER WITH VARIATION OF 'k'
k=0
k=0.5
k=0.75
GAIN (dB)
10
0
-10
-20
-30
-40
FREQUENCY (kHz)
0
10
20
30
40
50
60
70
80
90
100

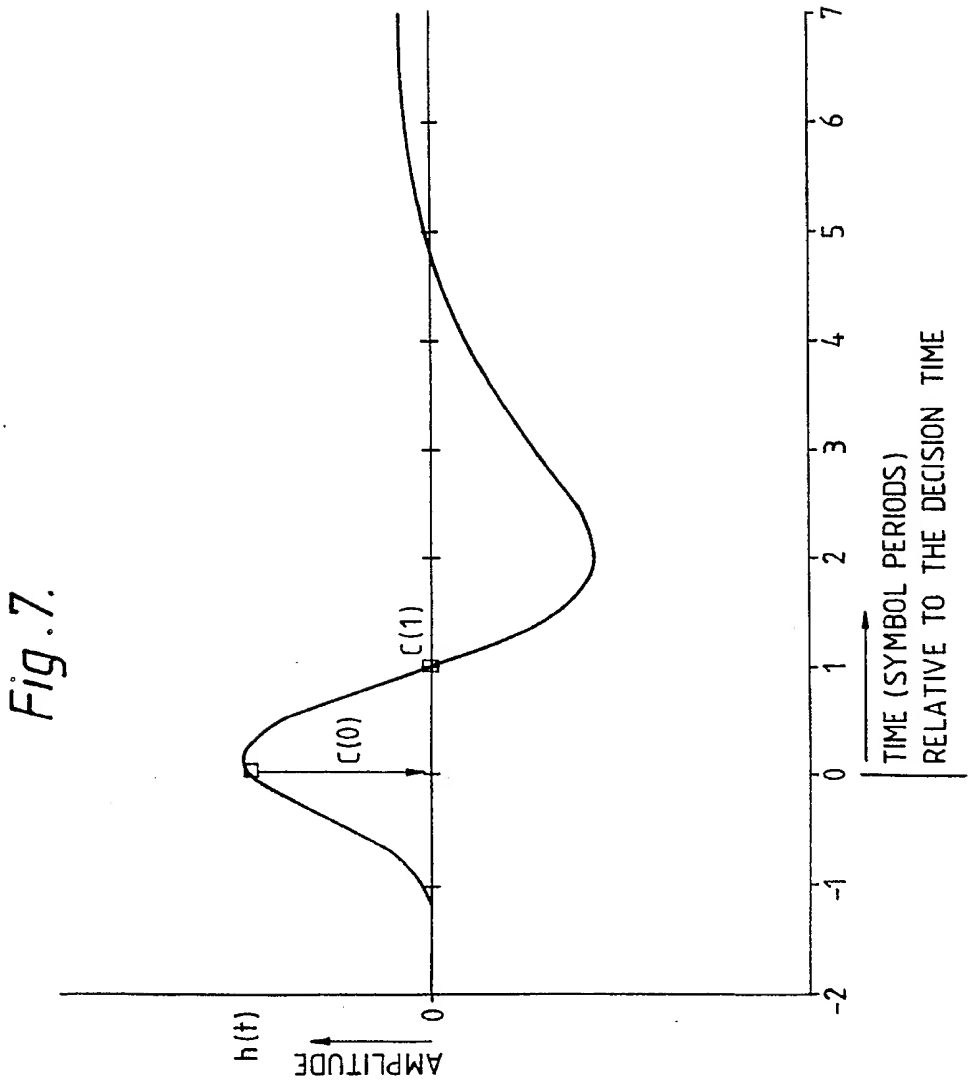

h(t)
AMPLITUDE
0
C(0)
C(1)
-2
-1
0
1
2
3
4
5
6
7
TIME (SYMBOL PERIODS)
RELATIVE TO THE DECISION TIME

Fig. 7.

Fig.8.

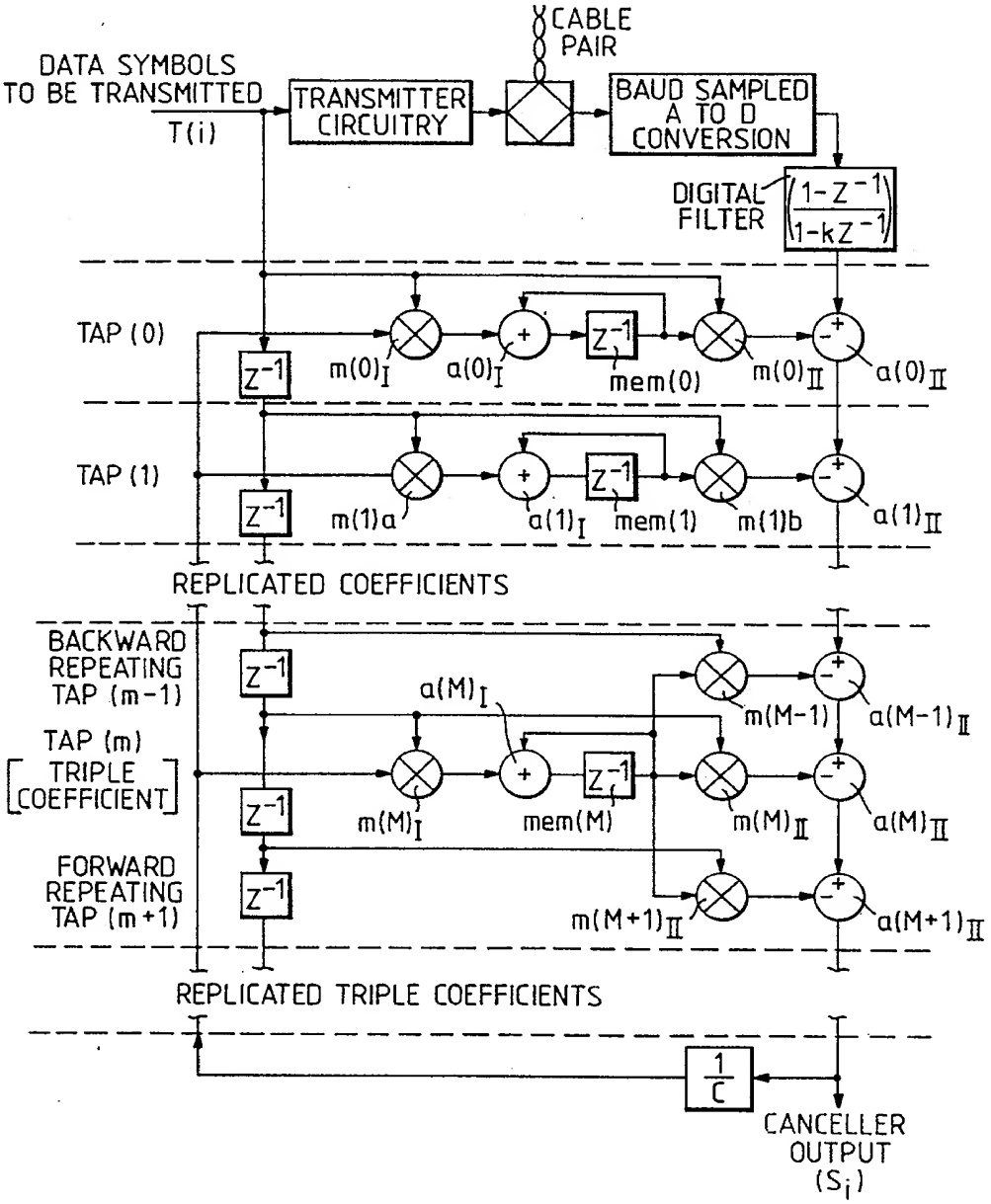

CABLE PAIR
DATA SYMBOLS TO BE TRANSMITTED
T(i)
TRANSMITTER CIRCUITRY
BAUD SAMPLED A TO D CONVERSION
DIGITAL FILTER
$\frac{1-Z^{-1}}{1-kZ^{-1}}$
TAP (0)
TAP (1)
Z^{-1}
$m(0)_I$
$a(0)_I$
mem(0)
$m(0)_{II}$
$a(0)_{II}$
m(1)a
$a(1)_I$
mem(1)
m(1)b
$a(1)_{II}$
REPLICATED COEFFICIENTS
BACKWARD REPEATING TAP (m-1)
TAP (m) TRIPLE COEFFICIENT
FORWARD REPEATING TAP (m+1)
$a(M)_I$
$m(M)_I$
mem(M)
$m(M)_{II}$
$a(M)_{II}$
m(M-1)
$a(M-1)_{II}$
$m(M+1)_{II}$
$a(M+1)_{II}$
REPLICATED TRIPLE COEFFICIENTS
$\frac{1}{C}$
CANCELLER OUTPUT (S_i)

Fig. 9.

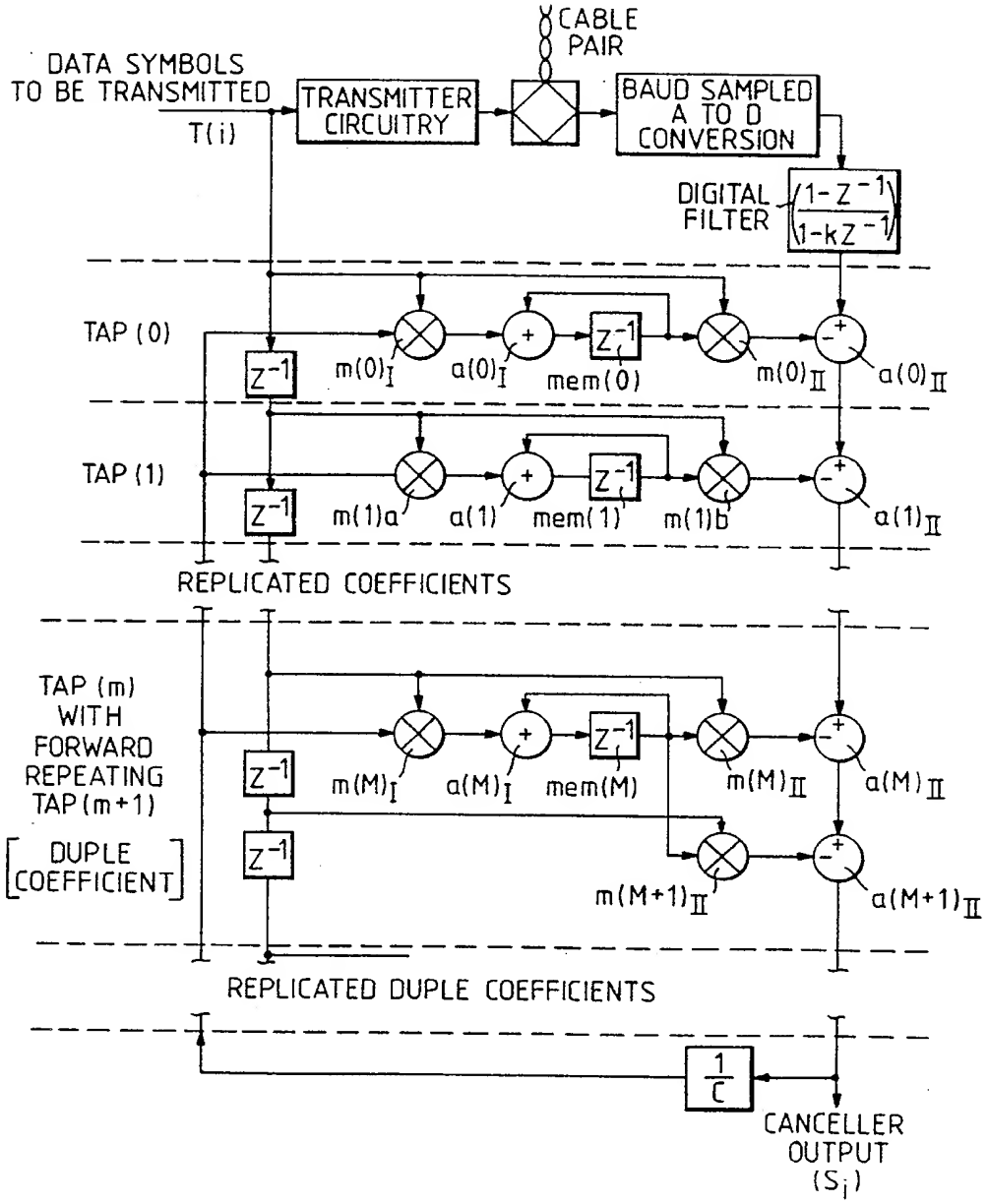

CABLE PAIR
DATA SYMBOLS TO BE TRANSMITTED
T(i)
TRANSMITTER CIRCUITRY
BAUD SAMPLED A TO D CONVERSION
DIGITAL FILTER
(1-Z⁻¹)/(1-kZ⁻¹)
TAP (0)
Z⁻¹
m(0)I
a(0)I
mem(0)
m(0)II
a(0)II
TAP (1)
m(1)a
a(1)
mem(1)
m(1)b
a(1)II
REPLICATED COEFFICIENTS
TAP (m) WITH FORWARD REPEATING TAP (m+1)
DUPLE COEFFICIENT
m(M)I
a(M)I
mem(M)
m(M)II
a(M)II
m(M+1)II
a(M+1)II
REPLICATED DUPLE COEFFICIENTS
1/C
CANCELLER OUTPUT (Si)

Fig.10.

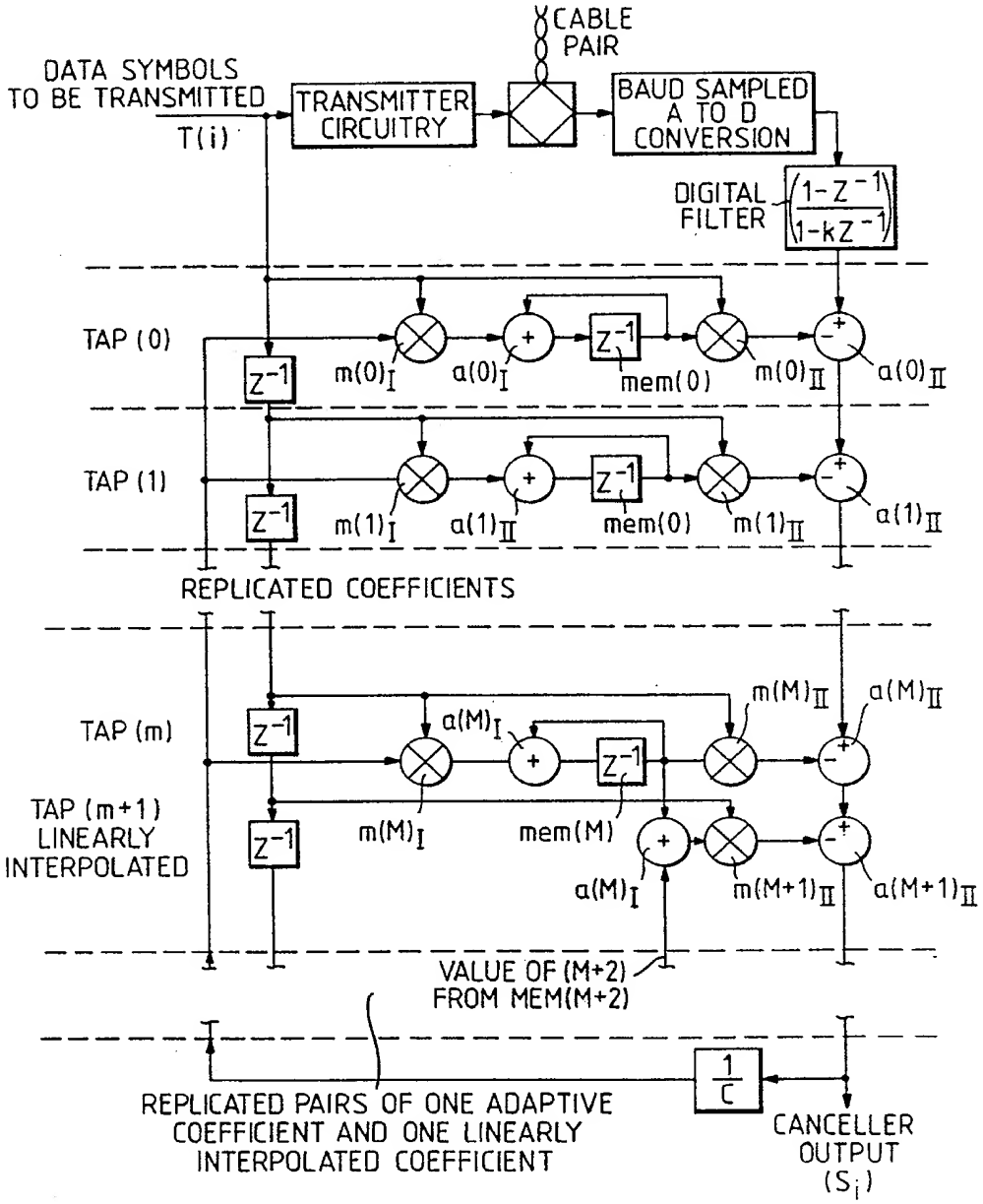
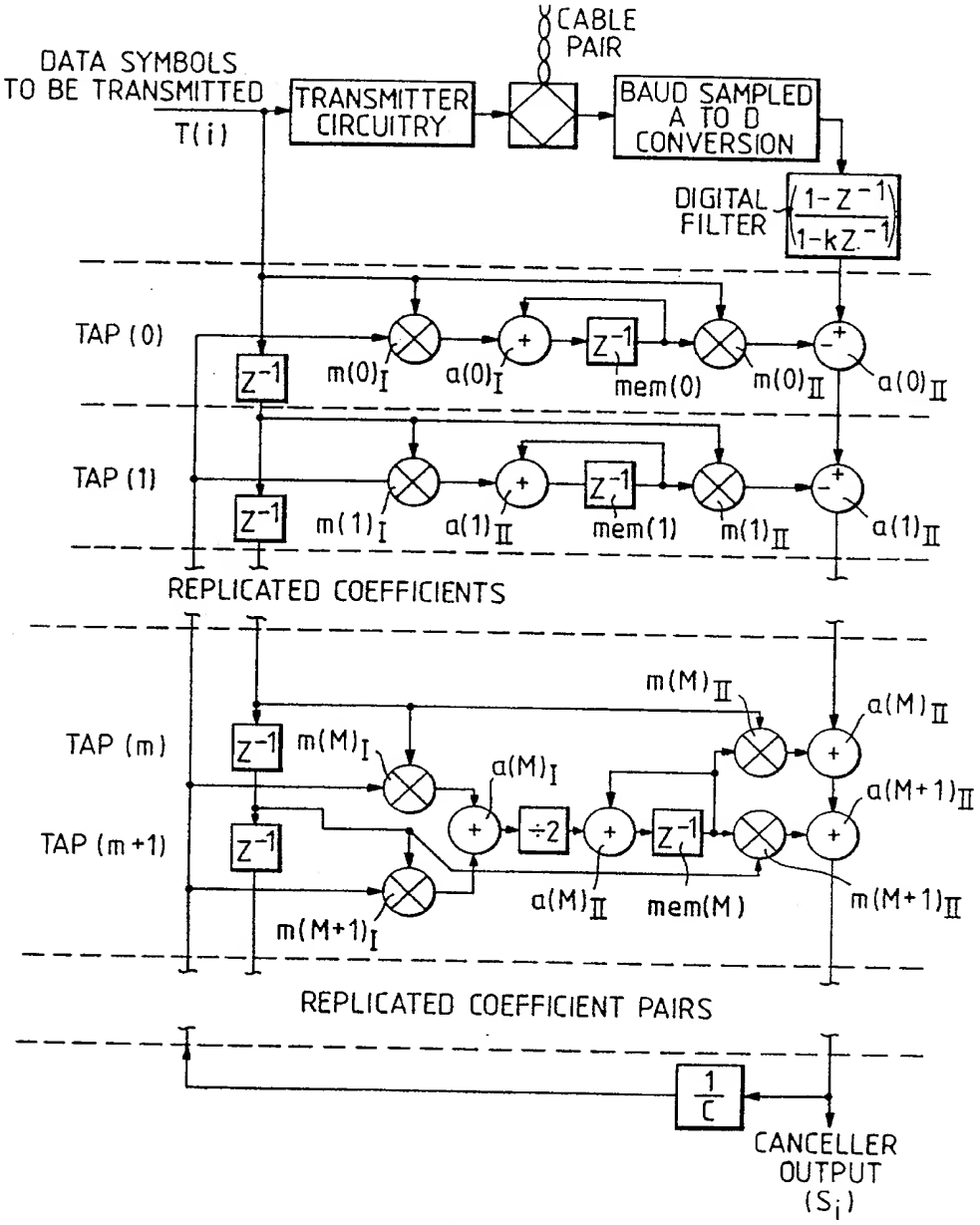

CABLE PAIR
DATA SYMBOLS TO BE TRANSMITTED
T(i)
TRANSMITTER CIRCUITRY
BAUD SAMPLED A TO D CONVERSION
DIGITAL FILTER
TAP (0)
TAP (1)
TAP (m)
TAP (m+1) LINEARLY INTERPOLATED
REPLICATED COEFFICIENTS
VALUE OF (M+2) FROM MEM(M+2)
REPLICATED PAIRS OF ONE ADAPTIVE COEFFICIENT AND ONE LINEARLY INTERPOLATED COEFFICIENT
CANCELLER OUTPUT (Si)

Fig. 11.


CABLE PAIR
DATA SYMBOLS TO BE TRANSMITTED
T(i)
TRANSMITTER CIRCUITRY
BAUD SAMPLED A TO D CONVERSION
DIGITAL FILTER
(1-Z⁻¹)/(1-kZ⁻¹)
TAP (0)
TAP (1)
TAP (m)
TAP (m+1)
Z⁻¹
m(0)I
a(0)I
mem(0)
m(0)II
a(0)II
m(1)I
a(1)II
mem(1)
m(1)II
a(1)II
REPLICATED COEFFICIENTS
m(M)II
a(M)II
m(M)I
a(M)I
÷2
a(M+1)II
a(M)II
mem(M)
m(M+1)II
m(M+1)I
REPLICATED COEFFICIENT PAIRS
1/C
CANCELLER OUTPUT (Si)

DATA TRANSMISSION SYSTEM

BACKGROUND OF THE INVENTION

This invention relates to a data transmission system, and is described herein as applied to a full duplex 144 Kb/s subscriber loop transmission system.

The present invention relates to an improvement of the invention of British Published Appln. No. 2161676A.

That application describes a data transmission system in which the data to be transmitted is in digital form, and is transmitted over the line in an analogue form. To maintain synchronization between the ends of the system a pilot tone is sent in addition to the data, this pilot tone having an amplitude which is small compared with that of the data signal. The pilot tone frequency has a fixed and known relation to the data bit rate, e.g. one-half of that bit rate. Thus the addition of the pilot tone does not increase the bandwidth. Sampling of the data signal is effected under the control of the local clock, and adjustment of that local clock is effected in response to the detected pilot tone. This detection occurs concurrently with the sampling and detection of the data signals, and the local clock is compared with the received and detected pilot tone, the timing of the local clock being adjusted in accordance with the results of that comparison to maintain synchronism.

SUMMARY OF THE INVENTION

An object of this invention is to provide improvements on the system of the above-mentioned Application.

According to the present invention there is provided a data transmission system in which the data to be transmitted is in digital form and each digital bit thereof is transmitted over the line in an analogue form, in which to maintain synchronization between the ends of the system a pilot tone is sent with the data, which pilot tone as transmitted is also in analogue form and has an amplitude which is small compared with the amplitude of the data signal, in which the pilot tone frequency has a fixed and known relation to the data bit rate, so that adding the pilot tone causes little or no increase in bandwidth, in which sampling of the data signal at the receiving end is under control of a local clock, adjustment of which is effected in response to the detected pilot tone, which detection is effected concurrently with that of the data signals, in which to effect said adjustments the local clock is compared with the received and detected pilot tone, the timing of the local clock being adjusted in accordance with the results of said comparison to maintain synchronization, and in which the receiving path at the receiving end includes in sequence a low-pass filter to which the received symbols are applied from a hybrid connected to the line, a sample and hold circuit which determines the values of the symbols and operates under the control of the local clock, an analogue-to-digital converter to which the output of said sample and hold circuit is applied, and a high-pass filter to the input of which is applied the output of the sample and hold circuit, the output of the high-pass filter being applied to one of the inputs of a subtractor to the other input of which is applied an input from an echo simulator.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention will now be described with reference to the accompanying drawings, which show the application of the invention to a 144 Kb/s subscriber's loop. In these drawings:

FIG. **1** is a simplified block diagram of the master station of the system of the above identified British Application, which includes details of pilot tone addition.

FIG. **2** is a simplified block diagram of the slave station of the system of the above identified British Application, to which the invention is applicable and which includes details of the pilot tone extraction method.

FIG. **3** is a waveform diagram showing the relation between data, data clock, pilot tone clock and pilot tone waveforms.

FIG. **4** shows a modification to the arrangement of FIG. **1** so as to include a high-pass filter in the transmitter.

FIG. **5** shows a possible implementation of the high-pass filter of FIG. **4**.

FIG. **6** is an explanatory graph, which is referred to later.

FIG. **7** is a plot of the transmission symbol response seen at the equalizer input.

FIG. **8** an implementation of the echo canceller using 'triple' coefficients incorporating interpolation.

FIG. **9** is an implementation of the echo canceller using 'duple' coefficients incorporating interpolation.

FIG. **10** is an implementation of the echo canceller using linearly interpolated coefficients.

FIG. **11** is an implementation of the echo canceller where the coefficient value is adapted to the mean value of two adjacent sampling instants.

DESCRIPTION OF PREFERRED EMBODIMENTS

The system has two ends, the master end with a master oscillator which controls the PCM transmission rate, and a slave end synchronized to the master end by a clock synchronization circuit. Where the system is used for a telephone subscriber's loop, the master end is at a telephone exchange, usually as part of a subscriber's line circuit, while the slave end is at the subscriber's instrument. There are two modes of operation of such a system, training and steady state. The steady state mode is simpler and is described first.

During steady state operation, pilot tone transmission only occurs from master to slave and the master end sampling phase is fixed. The signal flow in this direction is described with reference to FIGS. **1** and **2** which show schematically the transmitter and slave receiver component parts of the echo cancelling transmission system. In the reverse slave to master direction the pilot is only used during training and the slave pilot transmission circuit and master pilot recovery circuits are inoperative.

The transmitter circuit for the master station is shown in FIG. **1**. In this case the data baud rate as transmitted is $f_o = 100$ kHz, and ternary non-return to zero pulse shaping is used. The relationship between the data clock of frequency $f_o = 100$ kHz and sample data is given in FIGS. **3A** and **3B** respectively. The code employed is 3B2T, as in U.S. Pat. No. 4,539,675 (D. A. Fisher), except that the synchronization word in the present case has five symbols occurring every 120 data symbols

and is either 11110 or 11112, assuming the same symbol notation as in the patent specification just mentioned.

The pilot tone, FIG. 3D, is a squarewave of frequency $f_o/2=50$ kHz, and the phase relationship between the data and the pilot tone is such that transitions of the pilot each occurs at the mid-point of a data bit element. The pilot tone clock is shown in FIG. 3C and the pilot tone is produced by dividing the pilot tone clock by two. In general, the PCM data signal shape must have even symmetry, and at the point of addition the zero crossings of the $f_o/2$ pilot tone must coincide with the centres of the transmitted PCM signal shapes. In addition, the pilot tone must have odd symmetry about its zero crossing and must contain energy at the half symbol rate.

Addition of the pilot tone to the PCM data is done either in the analogue domain using an operational amplifier as in FIG. 1, or in the digital domain using for example, a twos complement number representation of the data signal and pilot amplitude.

The peak amplitude of the pilot tone is one quarter of that of the PCM data signal at the point of addition in the 144 kbt/s subscriber loop case. This ratio is not critical and is chosen to suit the parameters of the data receiver and data channel.

A low pass filter is placed between the pilot addition circuit and the line coupling circuit to control the transmitted data spectrum so as to limit interference. This low pass filter may be either a linear phase or minimum phase design with either analogue or digital implementation. With a digital implementation a digital to analogue converter is needed to generate the signal for transmission. The composite signal is then transmitted onto the cable via a linear resistive hybrid.

We now consider FIG. 1 in more detail. The incoming data signal is applied to a data encoding/scrambling arrangement 1 which eliminates auto-correlation in the transmitted data and cross-correlation between the two directions of transmission. The encoding produces an output in ternary form at 100K baud, which corresponds to 144 kb/s binary form plus frame synchronization. This output is applied to two data latches (D1) and (D2), one (D1) for data sign and the other (D2) for data magnitude. The outputs of these two latches control a three-level digital/analogue converter 2, the output of which passes via a resistor R1 to one input of an operational amplifier 3.

The pilot tone is derived from the pilot clock, which runs at 100 kHz (and is phase-locked thereto), via a divide-by-two circuit 4 the output of which goes to a two-level digital-to-analogue converter 5. The output of this converter 5 is applied via another resistor R2 to the amplifier 3, so that the pilot tone is added to the data signal. The combined signal is applied via a low pass filter 6 to a resistive hybrid 7, and therefrom to the line.

In the incoming direction the received signal is applied via the hybrid 7 to a receiver block 8. This includes input filtering, and analogue-to-digital conversion, with baud-spaced sampling whose control is described later.

The output of the block 8 goes to an echo and pilot simulation and cancellation block 9, which has a second input from the outgoing or GO path. This echo cancellation is needed because in practice the hybrid is imperfect and allows some break through of the GO signal to the receive side. This second input enables the breakthrough signal to be cancelled.

The output from the block 9 goes to the block 10, which provides equalization, and detection of the time at which sampling should be effected. The result of this detection controls the block 8 via the sample time control loop connection. The output from the block 10 goes to a data decoding and descrambling block 11 the output of which is the 144 Kb/s data.

The echo canceller operates as in U.S. Pat. No. 4,539,675 above. Here, however, the relation between the transmission clock and the receiver clock at the master end is frozen before the echo canceller is activated. This avoids the need for circuitry to cater for the cancellation discontinuity which occurs when the canceller data input clock and receiver sample cock cross over. The structure of the block 9 is modified to include an adaptive coefficient to eliminate the locally generated pilot tone. The method of adaption and the rate of adaption of this coefficient is as used for the other coefficients, and adapts the coefficient by an assessment proportional to the estimated gradient of the coefficient error.

This echo simulator generates a signal to be subtracted from the received signal, which signal corresponds to the transmitted signal. The simulator is an adaptive transversal filter having coefficients 1 to n and includes delay elements Z^{-1}, Z^{-2}, . . . Z^{-n}, one for each of a number of previous bits. Each element feeds the combination of a first multiplier, an accumulater and a second multiplier. Each accumulator has a forward delay Z^{-1}.

The coefficient values are stored in the delay elements (Z^{-1}) a twos complement number, and are multiplied by the delayed data symbols using the second multipliers and summated in a summation circuit whose output goes to a subtractor. The subtractor output provides the canceller output sample to the equalizer. This sample is scaled by 1/C and correlated with the corresponding symbol values in the first multipliers and used to increment the coefficient values stored in the delay elements.

During steady state operation, the canceller only has to track small changes in the substantially time invariant transhybrid impulse response. In this case the established sign updating variant of the adaption algorithm is appropriate, whereby the coefficient value is incremented or decremented by its least significant bit dependent only on the sign of the first multiplier product. This reduces the coefficient accumulator to an up-down counter.

The locally generated pilot tone is cancelled by another coefficient generation circuit. This has its first multiplier "driven" by the output of the subtractor via the scaler, as for the other such circuits, but its other input to its multipliers comes from the local pilot tone. Thus the difference between this and the other coefficients is that the delayed transmitted data input to the multiplier is replaced by an input toggled at the pilot tone frequency of 50 KHz.

We now turn to FIG. 2, which includes more detail of the receive circuitry used at both stations. Here the local transmitter 21, from which data signals to be sent to the remote station come, is connected to the hybrid 22, and also for echo cancellation purposes to an adaptive echo simulator 23. The output of this goes to a subtractor 23A which subtracts the "simulated" version of the outgoing data from the incoming signal from the loop.

The incoming signal passes from the hybrid **22** via a low pass filter **24** to a sample and hold circuit **25**, which samples each incoming data bit under control of a sample time controller **26**. The output from the circuit **25** goes via an analogue-digital converter **27** and a high pass filter **28** to the subtractor **23A**. The output of this goes to an automatic gain control circuit **35**, whose output goes via an adaptive precursor equalization block **29** to a block **30**. As will be seen, one improvement made by the present invention relates to the high-pass filter.

Block **30** is an adaptive decision feedback equalizer and pilot tone eliminator, and has an input from a pilot tone phase reference circuit **32**. The output from the block **30** forms one input of a mode selector **31**, which input is used during normal operation. During steady state operation at the slave station, the mode selector **31** connects the output of the block **30** to the sample time controller **26**. Hence the block **30** controls the sampling times for the receive side of the slave end.

The receiver also includes a "wake-up" detection circuit **33**, which responds to incoming signals, and is analogous to the conventional telephone bell.

The receiver also includes a "training" pilot phase detector **34**, which determines incoming pilot tone phase from what the slave receives. This it does with reference to the local pilot phase reference **32**, and the result of its detection is applied when in the training mode via the mode selector **31** to the controller **26**. Hence this is effective when setting up the loop circuit.

The timing extraction circuit in the block **34** adjusts the time at which the composite received signal is sampled by the circuit **25**, preceding the converter **27**.

In the steady state mode data transmission and timing extraction have been set up in both directions. Data plus pilot tone passes from MASTER to SLAVE and data only from SLAVE to MASTER. The slave end sampling phase is determined by dividing the frequency generated by the slave end crystal oscillator (not shown), which in this case is 12.8 MHz, by 128 to give the 100 kHz. The slave end receiver sampling clock is always coincident with the slave end transmission clock.

The slave crystal oscillator frequency may drift with respect to the MASTER end oscillator, so to keep the clocks in synchronism it is necessary to periodically extend or reduce the time between the 100 kHz clock rising edges. Thus if the sampling phase has advanced relative to the incoming data the period between the clock cycles is extended to 129 cycles of the 12.8 MHz clock, while if the sample clock is retarded the period is reduced to 127 clock cycles. This extension or reduction is made following the sampled input which when processed by the slave echo canceller contains the first significant non-zero component of the transhybrid impulse response convolved with the final zero amplitude symbol of the frame synchronization word. The synchronization word is both unique and contains several consecutive zero symbols.

For those samples immediately following a simultaneous shift in the transmit and sample time at the slave end, the echo estimate made by the echo canceller is in error by the sum of the convolution of the transmitted data with the differential of the transhybrid impulse response with respect to the phase change. The first four terms in the differential of the transhybrid impulse response contribute much of the error, and can be removed by the cessation of transmission for a short period by sending zero amplitude symbols. A synchronization word containing four consecutive zero amplitude symbols which occurs every 125 symbols is selected as it is well matched to the 144 kbt/s subscriber loop application with phase shifts of 1/128 symbol periods.

The direction of adjustment of sampling phase is determined by whether at the sampling point the pilot tone zero crossing precedes or follows the sampling point. The timing extraction adjusts the position at which the signal is sampled to the point at which the pilot tone waveform crosses zero.

We now consider the start-up and training mode briefly. It is first necessary to "wake up" the system and to synchronize the two ends so that a known program of simplex transmission bursts may be used whereby each end knows when to transmit and when to receive.

This "wake up" signalling can use simple transmitted tones and be detected by tuned threshold comparison. One implementation uses a wake up signal using repetition of the sequence $++--$. This is detected by feeding the A to D converter output through a filter of response $(1-Z^{-2})$ then summing the resultant output over 8 input samples after which the sum is compared with a threshold. "Wake up" is valid if four consecutive summations exceed this threshold.

The slave end start up sequence control is started from the time at which the wake up signal summation drops below the "wake up" threshold. For slave end call initiation an identical "wake up" signal is transmitted in the slave to master direction and the same detection technique used. The slave end then waits for a return master to slave "wake up" signal for synchronization, see above. After "wake up", a pilot tone is transmitted from master to slave end for 512 symbol periods. At the slave end adjustment of the sampling phase is made, taking one phase step of amplitude 1/32 symbol periods every 16th symbol. The pilot is then transmitted by the slave to the master end for the same duration. The master end thus adjusts its sampling time in an identical manner to the slave and then locks this phase value relative to its transmission phase.

A second cycle of adjustment may then be used in which the pilot tone is transmitted for 512 symbol times each way in succession with phase steps of 1/128 to fine tune the timing. Thus rapid phase acquisition occurs, which at the exchange end needs no further adjustment for the remainder of that connection.

There then follows a training period in which one burst of data is sent each way simplex. Training data plus pilot is transmitted from master to slave and during this period the master canceller is trained with the slave equalizer and slave timing extraction operated. Without the remote signal, canceller coefficient perturbation is reduced and the scaler determining the canceller adaption rate (1/C) can be increased to a high value for example 1/256. Simultaneously the slave equalizer receives the data signal and pilot and the equalizer coefficient adaption is enabled following a period for AGC stabilisation.

The direction of binary data transmission is then reversed, but the pilot remains in the master-slave direction and the slave equalizer continues to enable adaption of its pilot tap whilst always making decisions of value zero thus disabling its other coefficients. Thus timing extraction is maintained in the master slave direction controlled by the pilot coefficient sign as defined previously. Adaption of the slave end canceller and master end equalizer is then enabled for the same duration as

the previous training burst Perturbation of the slave canceller coefficients due to the presence of the remote but low level pilot has no significant effect on their accuracy.

Following these two simplex periods steady state full duplex operation with multi-level codes can commence. The canceller adaption is enabled at a much slower rate using for example the sign only adaption algorithm.

The master station end circuitry and the slave station circuitry can each be implemented in integrated circuit form, when it may be desirable for a "standard" chip to be used which involves the circuit elements common to both the master and the slave station.

We now discuss the modifications to the arrangements provided by this invention. These relate to a number of aspects. The first is an improvement in the use of the synchronization words at the subscriber end, which doubles the effective length of the word in relation to its ability to suppress the transient echo canceller error due to a small step in the sampling time of the A-to-D converter. The second aspect relates to the definition and position of the high pass filter, block 28, FIG. 2. This performs three functions, (a) DC offset elimination, (b) shortening of the tail of the pulse response and (c) filtering the received signal and noise components. Further, it may be at the transmitter or receiver or divided therebetween, so that sensitivity to noise, the amplitude distribution of the transmitted signal and the frequency spectrum of the transmitted signal can be modified to suit the specific operating environment.

The third addition is an improved way in which the pilot coefficient is used as a phase discriminator to control the digital phase-locked loop. The fourth addition is an alternative arrangement for providing for improved control of the digital phase-locked loop driven from the pilot coefficient. The fifth addition is an alternative to the use of the pilot coefficient for control of the digital phase-locked loop, which avoids use of the pilot after training and is applicable to master or slave ends of the system. It is essentially a variation of the tracking method described in U.S. Pat. No. 4,539,675, but using the pilot to initially locate the tracking point. The sixth addition is an alternative structure for the adaptive filter coefficients used for the echo canceller and equalizer, which reduces the volume of circuitry needed to provide for a similar degree of echo cancellation or equalization by the interpolation of taps used to represent the decaying tail of the transhybrid or transmission impulse response.

We first consider the first of these aspects. In a system as described, echo cancellation is used, whereby the transhybrid signal components of a known data sequence being sent to the far end of a cable are removed from the received data signal by subtraction. This is done numerically using logic circuitry. The transmitted data is superimposed on the received data as in the transmission scheme described above and in U.S. Pat. No. 4,539,675.

At the subscriber end the echo canceller consists of an adaptive transversal filter, i.e. the echo simulator, block 23 of FIG. 2, into which the source data is input. This takes one input for every transmitted data symbol and produces at its output the convolution of the data sequence and the adaptive filter coefficients.

There is a parallel signal path (the transhybrid path) whereby the data symbols to be transmitted are shaped and converted to a continuous signal using a digital-to-analogue converter and transmitted onto the cable through a hybrid. This hybrid also simultaneously receives the signal from the exchange end, which signal is then converted to a sampled data signal by circuits equivalent to a low pass filter, sample and hold circuit and A-to-D converter. The output from the converter is 12 bit digital words at a frequency equal to the nominal symbol rate of the exchange end transmitter.

Before 'echo cancellation' the signal passes through a high pass filter of the form $(1-Z^{-1})/(1-kZ^{-1})$ where Z^{-1} represents a one symbol period delay. This filter is described in more detail below, and preferred values of k are 0.5 or 0.75.

The components of the unwanted local signal estimated by the echo simulator are subtracted from the output of the high pass filter, this being echo cancellation. All unwanted interference due to the transmitted signal is removed, if the coefficients of the echo simulator match the pulse response of the transhybrid signal path. However, as the crystal oscillator at the slave has a small frequency offset with respect to the master oscillator, to keep the clocks in synchronism, a digital phase locked loop may be used. In this case a symbol period clock used to select the sampling time and transmitter time is made by dividing the slave/subscriber crystal frequency by a nominal divisor, 128 in this case. This number of cycles is extended or reduced by one according to the sampling time control circuitry to maintain the slave sampling in track with the master transmitted data.

The first echo simulator estimate following a simultaneous time shift in the transmitter clock and sampling time clock at the slave end, will be in error by the convolution of the data sequence sent to the cable immediately prior to the time shift with the differential of the transhybrid pulse response over the time shift. Calculation shows that with a time shift of 1/128 symbol periods, this interference can cause occasional errors to the received data with a cable pulse attenuation of 30 dB. The interference thus generated decreases with successive data periods because data symbols transmitted following the phase step have the same relationship to the new A-to-D sampling time as existed before the phase step. Only the relationship between data symbols transmitted before the phase step and the A-to-D sampling time after the phase step has changed.

This problem is overcome by changing the sampling time only after the transmission of a sequence of zero elements. This zero valued data is a word also used for frame synchronization. Clearly a similar result could be obtained if the line code was one in which strings of zero valued data symbols occur.

An additional immunity to the effect of the noise remaining due to a phase step in the receiver sampling time and transmitter clock may be realised by additionally aligning this change with the reception of the first zero of the synchronization word being received. The burst of noise due to a step in sample time depends on the differential of the transhybrid response over the step increment convolved with the data being transmitted. Thus a great deal of this noise may be eliminated as described by aligning the transmission of a sequence of zero elements in the form of synchronization words with the phase step. However, with too short a sequence of zeroes some noise component may remain due to the phase step, the amplitude of which depends on the data sequence which for the 3B2T code defined is scrambled and so random. Thus there is a small possi-

bility with a minimum length synchronization word that this noise occasionally exceeds a threshold sufficient to cause an error in the detection of a data element. However, if the data element being received is known or predictable with a high degree of certainty, as for the synchronization word, an error introduced occasionally into the reception thereof can be detected, but over-ridden in terms of the decision fed back into the decision feedback equalizer. It is thus prevented from propagating further errors due to the decision feedback process. The correct detection of a synchronization word in the correct location in the data sequence is used to increment a 'confidence count' in the frame synch. verification circuitry. An error event detected as described decrements the 'confidence counter' so that if this counter is at zero, the location of the synch. word is considered lost, and a search mode commences. If the counter exceeds 4 synchronization is considered to be verified. An upper limit of 63 is set on the counter value, which value is not critical but selected to match the time constants of the system.

The equalizer's ability to detect a decision that would have been incorrect due to a fore-knowledge of the location of the synchronization word in the data sequence, and so a count of correct versus incorrectly received synchronization words, can still be maintained to ensure confidence in the position of the synchronization word despite its use to prevent error propagation.

This technique is applicable only to the slave end where phase steps occur simultaneously with the transmitter clock and the receiver sample time. It is also advantageous to initially defer attempting to qualify frame synchronization at the master end of the system for a brief period at the start of ternary transmission because one has to shift the position of the synchronization word transmitted from the slave to align it with the correct position of the received synchronization word after having started transmission without this knowledge in a random position. Alternatively, synchronization can be achieved prior to ternary transmission by introducing signals into the binary training sequences or by deferring the transmission of ternary in the slave to master direction until the slave achieves frame synchronization.

Note that the technique can also be used at the master end to over-rule a burst of errors that might occur while receiving the synchronization word and thus help to prevent error extension in the decision feedback equalizer, this being known.

We now consider the definition and location of the high-pass digital filter with respect to FIG. **4**. After the data to be transmitted is encoded as described, it is fed into a pulse shaping circuit **41**. This circuit behaves as a finite impulse response filter acting at a rate N times the symbol rate excited by symbols of width 1/N symbol periods of amplitude +1,0 or −1. In the simplest case this filter produces a rectangular pulse one symbol period wide. However to control the transmitted signal spectrum a more complex pulse shaping circuit is used. This generates for an isolated '1' a pulse with even symmetry and typically with a spectrum which (after replicated side band removal) is constrained between DC and a frequency exceeding the half baud rate of the data but in general below a quarter of the sampling frequency of the pulse shaping filter.

The pilot tone generation circuit **42** produces a tone which in the simplest case is a continuous series of alternating data elements +1, −1, whose transitions occur in the centre of the even symmetric data pulses. This could be filtered as in FIG. **1**. Alternatively in a digital implementation, the pilot tone can be generated as a series of discrete samples closely matching a pure sine wave.

We now consider with reference to FIG. **4** a simple implementation of the transmitter side, which differs from that of FIG. **1**. Here the source data S_i is applied via pulse-shaping circuitry **41** to one input of an adder **43** to the other input of which is applied the output of a pilot tone generation circuit **42**. The output of the adder is applied via a filter **44**, of characteristics $(1-Z^{-1})/(1-hZ^{-1})$, which feeds a digital-analogue converter **45**, whose output is applied via a low-pass filter **46**, a line amplifier **47**, and hybrid **48** to the line. Although FIG. **4** shows a high-pass filter **44** in the simplest case such a filter may be omitted, as in FIG. **1**. When the filter is not used at the transmitter, the series of data values from the adder is fed directly to the D-to-A converter. Such a filter can, however, be used as shown in FIG. **4** to alter the properties of the transmitted signal. This will be described in more detail in combination with the description of the high-pass filter in the receiver.

In the simplest form of the system, the digital high pass filter is only included in the receiver path, block **28** in FIG. **2**. This filter is of the form $(1-Z^{-1})/(1-kZ^{-1})$ where Z^1 represents a one symbol period delay. The filter may be realised as shown in FIG. **5** using two delays each storing one word of data. The first circuit achieves the numerator function which is a differentiation over one symbol period of the received data. The second circuit performs the denominator function, a lossy integration of the output from the differentiator. The frequency response of the filter for values of $k=0$, $\frac{1}{2}$, $\frac{3}{4}$ is given in FIG. **6**. For $0 \leqq k < 1$, the filter eliminates from the received signal any DC component due to analogue-to-digital conversion and/or arithmetic truncation. A further important purpose of this filter is to increase the rate at which the tail of a transmitted pulse decreases, and so to reduce the number of taps in the echo canceller and equalizer.

With the value of $k=0$, the filter is as in U.S. Pat. No. 4,539,675 above, and the length of the echo canceller and equalizer is maximally reduced. There is a cost due to the increased sensitivity of the receiver to high frequency noise sources and near end crosstalk from like systems, The value of k which provides significant reduction in pulse length at a lower cost to performance is $k=0.5$ or 0.75.

The filter in the receiver may also be in the transmission path. In this case the receiver filter has a very long time constant. With the transmit filter having coefficient $h=\frac{1}{2}$, and the receiver filter having coefficient $k=63/64$ the overall pulse response at the output of the receiver high pass filter is similar to that obtained when only a receive filter of coefficient $k=0.5$ is used.

The advantage of locating this filter at the transmitter depends on the noise environment on the cable and the signal characteristics required on the cable. The peak excursion of the signal at the analogue-to-digital converter input compared to the amplitude of the epoch of the pulse being received from a similar remote transmitter is an important parameter. This is closely related to the crest factor of the received signal which is defined as the peak to RMS ratio of the waveform.

With filter coefficient $h=1$ at the transmitter, the transmitted symbol is a dipulse and the code spectrum

becomes equivalent to the well known code Alternate Mark Inversion and has identical properties. The crest factor of the signal at the A-to-D input is approximately 6 dB lower than for the unfiltered random ternary signal for the same size amplitude of the pulse epoch. With filter coefficient h=0.5 at the transmitter, low frequency components of the code are also considerably reduced and the crest factor of the transmitted signal will be reduced by approximately 3 dB compared to the case with unfiltered random ternary data.

The high pass filter can be split equally between the transmitter and receiver, with h=k=¾ as the filter coefficient to provide some reduction of the transmitter crest factor, whilst maintaining a degree of low frequency interference rejection at the receiver.

We now consider the use of the pilot tone coefficient to control timing extraction. Our above-quoted British Application No. 2161676A disclosed a technique whereby a pilot coefficient is introduced into the equalizer to act as a phase discriminator having an amplitude which increases with the timing offset from the ideal sampling instant. In that application, only the sign of the pilot coefficient was used at intervals defined by the frequency of the frame synchronization word, and the sampling time of the A to D converter stepped backwards or forwards by 1/128th of a symbol period.

An improvement in the accuracy of control and a reduction in phase jitter results by using a second order control whereby the phase step is proportional to the phase error estimated by the amplitude of the pilot coefficient. This however would introduce complexity. A significant improvement over the basic scheme can be obtained with only a small complexity penalty by one of the two following methods:

(i) A phase step is only taken if the value of the pilot coefficient goes beyond the range −P to +P at the time for the phase step. The step size is fixed as before at +1/128 of a symbol period. It is advantageous to reset the pilot coefficient to zero when a step is taken.

(ii) An accumulator is placed on the output from the pilot coefficient. Only if this accumulator goes beyond the range +A to −A at the time for the phase step is a step taken, in which case the accumulator is reset and the phase step direction corresponds to the sign of the accumulator.

We now consider an alternative to the use of the pilot tone once the system has been trained which enables the tone to be removed after training and/or provides for phase tracking at the exchange (master) end of the system. The procedure is as follows.

The training procedure specified in our above-quoted British Application No. 2161676A is followed up to the point where duplex transmission is due to commence. At this point the subscriber end timing will be tracking the exchange using the pilot tone and the exchange end timing will be locked to the sampling instant, this having been located by the simplex pilot tone sequence at the start of training.

The first post-cursor C(1) is then stored in a 12 bit register as a "reference" value. The sampling time of the A to D converter is then adjusted to maintain the value of the post-cursor coefficient at this "reference" value under the conditions of full duplex data transmission. Thus if the post-cursor coefficient C(1) exceeds the reference, the sampling time is advanced, and if the post-cursor coefficient becomes more negative the sampling time is retarded. This technique may be applied at both ends of the system and has much similarity with the techniques described in U.S. Pat. No. 4,539,675, except that the value of the coefficient maintained by the timing is not preset from the outset, but determined from the value corresponding to the pilot tone zero crossing located during the training period. The assumption made is that the symbol response of the transmission channel is of the form given in FIG. 7 with a substantially monotonic decrease in the region one symbol after the epoc of the pulse.

Implementation requires that the post-cursor coefficient be subtracted from the reference using for example 2's complement logic and that the value of this difference be used to control whether a step occurs and the step size and direction by the same techniques already described for controlling timing from the pilot coefficient directly.

We now describe a method of reducing the number of components needed in the echo canceller or equalizer to estimate the tail of the impulse response with as few components as possible.

It has been proposed that the use of a high-pass filter after the A to D converter or in the transmitter leads to a useful reduction in the number of taps required in the echo canceller for a given level of cancellation. The following defines why this is so and describes an alternative method to the use of the high-pass filter using tap interpolation on the tail of the impulse response The transhybrid response only is referred to in the following text but the techniques are equally applicable in the equaliser.

Let the impulse response h(t) of the hybrid response be defined at discrete time intervals T corresponding to a symbol period.

$$h(t=0)=h(0) \qquad h(t=T)=h(1) \quad \ldots \quad h(t=nt)=h(n)$$

Then if this response is high-pass filtered following A to D conversion by subtracting one sample from the next using the filter $1-Z^{-1}$ the hybrid impulse response after the filter becomes h(0), h(1)−h(0), h(2)−h(1), . . . h(n)−h(n−1).

Let there by M canceller taps k(0), k(1), k(2) . . . k(M−1) and if we assume the taps to be adapted to match the corresponding hybrid response, the uncancelled error remaining due to the finite number of taps will at worst be the sum of magnitudes of the pulse response at the sampling instants from time t=m to ∞. Without the high pass filter this will be:

$$\sum_{n=m}^{n=\infty} |h(n)|$$

With the filter these remainder terms become

$$\sum_{n=m}^{n=\infty} |h(n)-h(n-1)|$$

If the impulse response after M symbol periods is substantially a decaying exponential, then the difference terms will be less than the unfiltered terms, and thus when the filter is used the number of taps can be reduced for a given degree of tail cancellation.

The use of the high pass filter gives rise to a reduction in the number of taps required because tap truncation leads to uncancelled terms in the transhybrid response consisting of symbol spaced difference terms of the tail of the transhybrid response An alternative to the filter is

therefore an echo cancelling structure that leads to similar difference terms. Such a structure is shown in FIG. 8. For the purposes of this explanation consider the digital filter notionally eliminated by the value of k being set to one.

Two types of coefficient are shown, taps 0 to (M−2) have standard form. Tap (M) also has standard form but the value of tap (M) is also used for evaluation of the convolution sum in place of having separate adaptive taps for time (M−1) and (M+1). Thus the taps (M−1) and (M+1) are interpolated from tap (M) and consequently a multiplier, an adder and a coefficient memory are saved in each case. This combination of a conventional adaptive tap and two interpolated taps (a "triple tap") is then repeated until the uncancelled terms in the transhybrid response become negligible.

Thus with M−1 conventional taps (0 to M−2) and X triple taps, the canceller error due to interpolation is of the form:

$h(M) - h(M-1)$,	$h(M) - h(M+1)$	for the first triple tap.
$h(M+3) - h(M+2)$,	$h(M+3) - h(M+4)$	for the second triple tap.
$h(M+6) - h(M+5)$,	$h(M+6) - h(M+7)$	for the third triple tap.

With random data of value +−1 or 0 the worst case sum of canceller error due to interpolation and truncation with X triple taps and M−1 conventional taps will be:

$$\sum_{n=M}^{n=M+3X-1} |h(n) - h(n-1)| + |h(n) - h(n+1)| + \sum_{n=M+3X}^{n=\infty} |h(n)|$$

The left hand term is the sum of symbol spaced difference terms of the transhybrid response omitting every third difference and is thus smaller than the case with the differentiating filter described above. Sufficient triple taps would in practice be used to cause the right hand term to be negligible.

An example of practical application of such a structure would be where the high-pass filter is retained with a value of the denominator coefficient k=0.5. The number of conventional taps M=20 and the use of triple taps X=8. Thus the triple tap section replaces conventional taps **20** to **44**.

FIG. **9** shows an arrangement which is similar to that of FIG. **8**, but using "duple" coefficients in place of the triple coefficients of FIG. **8**. It functions in a similar manner to FIG. **8**.

Further structures of this type giving similar results are also possible. FIG. **9** has a structure where the same tap is used as the basis for interpolation of the following tap thus requiring more circuitry than the triple tap structure but giving residual terms as below eliminating every second difference from the residual error. With M standard adaptive taps and Y duple taps the worst case canceller error due to interpolation and truncation is:

$$\sum_{n=M}^{n=M+2Y-1} |h(n) - h(n-1)| + \sum_{n=M+2Y}^{n=\infty} |h(n)|$$

Further alternatives giving higher accuracy are:

(i) Interpolate the value of even numbered taps after the mth tap by addition of the two odd taps either side and division by two. $k(i)=K(i-1)+k(i+1)$ for i even only. (FIG. **10**).

(ii) After the mth tap use the same tap value for even and odd delays and adapt the tap value depending on the sum of the adjacent data values. The tap adapts to a value mid-way between the two ideal values such that k(i)=k(1+1)=(h(i)+h(i+1))/2. (FIG. **11**).

I claim:

1. A method for maintaining synchronism between a master terminal and a slave terminal of a digital data transmission system in which data is transmitted over a line between the terminals in analogue form, which method includes:

sending from the master terminal to the slave terminal a pilot tone additional to the data, the amplitude of the pilot tone being small compared with that of the data signal, the pilot tone having a frequency with a fixed and known relation to the data bit rate, so that adding the pilot tone does not increase bandwidth;

sampling the data signal received at the slave terminal under the control of a local clock;

detecting the pilot tone at the slave terminal concurrently with the sampling of the data signals;

comparing the local clock with the detected pilot tone and adjusting the timing of the local clock in accordance with the results of said comparison to maintain synchronization between the slave terminal and the master terminal;

reducing error occurrence in the received data by comparing the value of a received data symbol whose value can be safely predicted, as in the case of a synchronization word, with what it should be, and over-riding the value as received if it differs from the predicted value, and when such an error is detected using said detection to decrement a confidence measure value in a synchronization location and verification circuit, said confidence measure value being incremented in response to the correct detection at the correct time location of the synchronization word;

and employing said error occurrence reduction operation to protect the slave terminal when a phase step by the local clock is taken in addition to the transmission of a specifically zero valued frame synchronization word, from the slave terminal immediately prior to the phase step occurring, and reduce the effect of time phase steps on system performance.

2. A method as claimed in claim **1** wherein said sampling includes the steps of applying the received data signal to a hybrid connected to the line, applying the output of the hybrid to a low pass filter, applying the output of the low pass filter to a sample and hold circuit which determines the values of the symbols and operates under the control of the local clock, applying the output of the sample and hold circuit to an analogue-to-digital converter, applying the output of the analogue-to-digital converter to a first high pass filter, applying the output of the first high pass filter to one of the inputs

of a subtractor and applying an input from an echo simulator to the other input of the subtractor.

3. A method as claimed in claim 2 wherein at the transmitter side of a said terminal of the system the following steps are performed, namely;

applying the data and the pilot tone to respective inputs of an adder;

applying the outputs of the adder to a second high-pass filter;

applying the output of the second high-pass filter to a digital to analogue converter, and

applying the output of the digital to analogue converter to a respective hybrid connected to the line for transmission to the other terminal.

4. A method as claimed in claim 3, wherein the output of the digital to analogue converter is applied to the respective hybrid via a low-pass filter and a line amplifier.

5. A data transmission system which embodies the method of claim 3 in which the characteristics of said second high-pass filter are defined by the expression:

$$\frac{(1 - z^{-1})}{(1 - hz^{-1})}$$

6. A method as claimed in claim 1 wherein the adjustment of the local clock is made in a step manner, the direction of the adjustment being that appropriate to correct a detected discrepancy, and wherein said adjustment is only made if the value of a pilot tone coefficient in a pilot tone and decision feedback equalization circuit exceeds a present value.

7. A method as claimed in claim 6 and, only when a phase step is taken, including the step of resetting the pilot tone coefficient to zero.

8. A method as claimed in claim 1 including the use of an echo cancellation circuit in which a pilot tone coefficient is employed, and including the steps of connecting an accumulator to the output of the circuit which generates the pilot tone coefficient and adjusting the local clock only if the content of the accumulator exceeds a present value, and, in that case, resetting the accumulator to zero.

9. A method as claimed in claim 1, including the steps of establishing bit synchronism between the two terminals of the system on switch on, or in response to a loss of frame synchronization, by the execution of a training sequence during which said adjustment of the local clock is effected based on use of the pilot tone; terminating the transmission of the pilot tone when synchronism is attained and determining a coefficient for use in the slave terminal; and storing the coefficient in a memory for use as a reference for future maintenance of synchronization.

10. A method as claimed in claim 9 and in which the bit synchronism technique referred to is also used at the master terminal.

11. A method as claimed in claim 1, including the use of an echo canceller with a multiplicity of coefficients at each end of the system, and wherein a said canceller which includes a finite impulse response filter is used which models the transhybrid response as in the case of the canceller, or the transmission response as in the case of a decision feedback equalizer of the echo canceller, and includes coefficients which are derived by interpolation from adjacent coefficients which are adapted according to the gradient of the tap error.

12. A data transmission system which embodies the method of claim 1 in which each of said terminals is implemented in integrated circuit form.

13. A method for maintaining synchronism between the ends of a digital data transmission system in which data is transmitted over a line between the ends in analogue form, which method includes:

sending a pilot tone additional to the data, the amplitude of the pilot tone being small compared with that of the data signal, the pilot tone having a frequency with a fixed and known relation to the data bit rate, so that adding the pilot tone does not increase bandwidth:

sampling the received data signal under the control of a local clock;

detecting the pilot tone with the sampling of the data signals;

comparing the local clock with the detected pilot tone and adjusting the timing of the local clock in accordance with the results of said comparison to maintain synchronization between the ends of the system;

performing echo cancellation operations upon the received data signal in echo cancellation circuitry including a decision feedback equalizer, the pilot tone being employed in said equalizer;

and, if the value of a pilot tone coefficient in said equalizer exceeds a present value, adjusting the local clock in a step-by-step manner, with the direction of the adjustment being that appropriate to correct a detected discrepancy.

14. A method as claimed in claim 13 and, only when a phase step is taken, including the step of setting the pilot tone coefficient to zero.

15. A method as claimed in claim 13 including the step of connecting an accumulator to the output of the circuit which generates the pilot tone coefficient and adjusting the local clock only if the content of the clock exceeds a preset value and, in that case, resetting the accumulator to zero.

16. A data transmission system which embodies the method of claim 13, in which each of said terminals is implemented in integrated circuit form.

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Related Proceedings Appendix

None